Limits to Binary Logic Switch Scaling—A Gedanken Model

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Invited Paper

In this paper we consider device scaling and speed limitations on irreversible von Neumann computing that are derived from the requirement of "least energy computation." We consider computational systems whose material realizations utilize electrons and energy barriers to represent and manipulate their binary representations of state.

Keywords*—*Closely packed devices, device scaling limits, digital integrated circuits, heat removal, nanotechnology, power consumption, tunneling.

I. SCALING PROJECTIONS

The explosive growth of digital information processing systems over the past 30 years has been driven by rapid scaling, first of a variety of integrated circuit technologies, and, more recently, by accelerated scaling of CMOS technology. Driven to obtain greater system functionality on chip, scaling of MOS transistors performing as simple electronic switches has been at the heart of this revolution. However, CMOS scaling will likely become very difficult at and beyond the 22-nm node (9-nm physical gate length). Consequently, new approaches are emerging for realizing similar switches in a variety of nanoscale technologies, including molecular structures, carbon nanotubes, silicon and germanium nanowires, etc. This paper addresses the question of the minimum size of any irreversible logic device that represents discrete binary logic states based on separation of a single charge for an arbitrary digital system executing the common von Neumann architecture.

There is a rich literature that offers perspectives on the limits of scaling [1]–[4], [11]. The question examined in this paper is: "What are the limits to the maximum speed, maximum density and minimum energy of a system of binary switches?" By using a simple physical model, we find that we are rapidly approaching the point where compromises are forced between device density and switching speed due to thermal constraints.

Two important parameters in the realization of digital systems are: 1) device switching time t and 2) integration density (number of binary switches per cm^2) n. Scaling has afforded continuous improvement in both of these parameters. As a result, the information throughput (e.g., the maximum number of binary transition per unit time $B = n/t$) has grown exponentially with time. Unfortunately, since each binary transition requires energy $E_{\rm bit}$, the total power dissipation growth is in proportion to the information throughput: $P = BE_{\rm bit}$.

Thus, to reduce power dissipation without sacrificing information throughput, $E_{\rm bit}$ must be decreased. The well-known minimum limit for $E_{\rm bit}$ is given by the *Shannon–von Neumann–Landauer (SNL)* expression for smallest energy to process a bit

$$E_{\rm bit} \geq E_{\rm SNL} = k_B T \ln 2 = 0.017\ {\rm eV} \quad (T = 300\ {\rm K}). \tag{1a}$$

If we endeavor to construct a model for a computer operating at SNL limit at 300 K, the minimum size and switching time of binary switches can be estimated based on the Heisenberg Uncertainty relations

$$\Delta x \Delta p \geq \hbar \tag{1b}$$

$$\Delta E \Delta t \geq \hbar. \tag{1c}$$

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From these equations, the minimum size $x_{\min}$ of a scaled computational element or switch, which operates at E_{SNL} is

$$\begin{aligned} x_{\min} &= \frac{\hbar}{\Delta p} \\ &= \frac{\hbar}{\sqrt{2m_e E_{\mathrm{bit}}}} \\ &= \frac{\hbar}{\sqrt{2m_e k_B T \ln 2}} \\ &= 1.5\ \mathrm{nm} \quad (T = 300\ \mathrm{K}). \end{aligned} \tag{2a}$$

This minimum size corresponds to a maximum integration density of switches

$$n_{\max} = \frac{1}{x_{\min}^2} = 4.7 \times 10^{13}\ \mathrm{devices/cm^2}. \tag{2b}$$

The minimum switching time of the gedanken least energy switch is estimated as

$$t_{\min} = \frac{\hbar}{\Delta E} = \frac{\hbar}{k_B T \ln 2} = 0.04\ \mathrm{ps}. \tag{2c}$$

The power dissipation per unit area of this limit technology is given by

$$P = \frac{n_{\max} E_{\mathrm{bit}}}{t_{\min}} = 3.7 \times 10^6\ \mathrm{W/cm^2}. \tag{2d}$$

If we let $E_{\mathrm{bit}} = K^* E_{\mathrm{SNL}}$, $K > 1$, then the feature size computed from (2a) will be smaller and the switching time will be faster, but unfortunately, the power per unit area at maximum packing density increases as K^3.

The 2001 International Technology Roadmap for Semiconductors (ITRS) calls for scaling of CMOS technology to the 22-nm node. This technology node specifies NMOS transistors with a physical gate length of 9 nm and a CMOS IC technology with a real gate density of $1.5 \times 10^9 - \mathrm{gates/cm^2}$ and power dissipation of 93 W/cm^2. The minimum-scaled computational switch discussed above has a minimum size only a factor of six less than the minimum size of the 22-nm node NMOS transistor (physical gate length of 9 nm), but has a device density 3×10^4 larger and a power density 5×10^4 larger than end-of-ITRS projections.

The size and switching time bounds and (1) and (2) are derived without reference to a particular device structure. Conceptually, the representation of a binary element requires a material system with two physically distinguishable states defined by the location of electric charge. Operation of the switch requires one to conditionally change the state of the material system. The usual approach to meeting these requirements is to utilize an energy barrier manifested in the material separating the binary states of the switch.

According to the Heisenberg/SNL model, it appears that reduced energy operation would occur with cryogenic temperatures. However, as will be shown in Section III, computing below ambient temperature requires additional energy for cooling, and the combined energy for computation will be larger than for computation at $T = 300$ K. In order to investigate the distinguishability and cryogenic operation questions, a more precise physical device model is required, which is described in the next section.

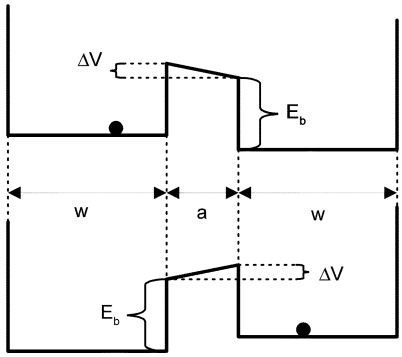

Fig. 1. Energy model for limiting device: w = width of left-hand well (LHW) and right-hand well (RHW); a = barrier width; E_b = barrier energy.

II. The Model: A Physical System as a Computing Medium

Classical information processing technology always requires a physical carrier, usually electrons and holes. The first requirement to physical realization of any arbitrary switch is the creation of *distinguishable* states within a system of such material particles. The second requirement is the capability for a *conditional* change of state. The properties of *distinguishability* and *conditional change of state* are two fundamental and essential properties of a material subsystem that represents binary information. These properties are usually obtained by creating *energy barriers* in a material system.

To that end, we consider a simple device consisting of two wells separated by a finite potential barrier, shown in Fig. 1. This device or switch has two stable states. Control of the switch operation (e.g., changing the electron position from one well to the other) is effected either by supplying the electron additional energy or, equivalently, by reducing the barrier energy, denoted by E_b. We assume that in the "on-state" the electron can move "freely" from one well to the other. However, in the "off-state" with the two wells separated by an energy barrier E_b, ideally there should be no movement of the electron between the wells. In real systems, there always is some probability (Π_{err}) of spontaneous transitions between the wells, and here we elaborate on the concept of *distinguishability*. The location of the electron is said to be "distinguishable" if there is a very low probability of spontaneous transition to the alternate well. If, on the other hand, for the election in a given state (well), the probability of spontaneous transition to the alternate state (well) is equal to 0.5, we say that distinguishability is lost. Thus, in the "off-state," $\Pi_{\mathrm{err}} = 0$ for an ideal, perfectly distinguishable switch state, and $\Pi_{\mathrm{err}} = 0.5$ for indistinguishable states. In "on-state," the probability of transition $P_{\mathrm{on}} = 1$.

We believe that the two-well, one-barrier model is a valid abstraction for electron transport switching devices. For example, the field-effect transistor (FET) can be thought of as consisting of two wells (source and drain) separated by a barrier (channel).

In this paper, we consider implications for device design at the highest levels of integration density and lowest levels of energy consumption. To a first approximation, the size of a switch is greater than a, while energy per switching operation is given by the barrier height E_b. The electron can spontaneously change state either due to classic overbarrier or quantum mechanical tunneling transitions. If the barrier width is large enough, only overbarrier transitions play a role, and the probability of such classic transitions is

$$\Pi_{\text{classic}} = \exp\left(-\frac{E_b}{k_B T}\right). \tag{3}$$

Solving (3) for $\Pi_{\text{classic}} = 0.5$, when distinguishability is completely lost, one obtains $E_b = k_B T ln2$, which is the well-known SNL energy limit per switch operation.

With respect to highest integration densities, when a is small, we argue that the Heisenberg Uncertainty relations give the limits of distinguishability. Consider again a "two-well" bit in Fig. 1. How close could the wells be to each other and still remain distinguishable? As is known from quantum mechanics, a particle can pass (tunnel) through a barrier of finite width even if the particle energy is less than the barrier height E_b. A simple analytical form of tunneling probability through a rectangular barrier is given by the Wentzel–Kramers–Brillouin (WKB) approximation [5]

$$\Pi_{\text{quantum}} = \exp\left(-\frac{2\sqrt{2m}}{\hbar} a\sqrt{E_b}\right). \tag{4}$$

Equation (4) also emphasizes the parameters controlling the tunneling process. They are the *barrier height* E_b and *width* a as well as the *effective mass* m. If separation between two wells a is less than the Heisenberg limit, the structure of Fig. 1 cannot represent a bit of information.

The total probability of spontaneous transitions is given by

$$\begin{aligned}\Pi_{\text{error}} &= \Pi_{\text{classic}} + \Pi_{\text{quantum}} - \Pi_{\text{classic}}\Pi_{\text{quantum}} \\ &= \exp\left(-\frac{E_b}{k_B T}\right) + \exp\left(-\frac{2\sqrt{2m}}{\hbar} a\sqrt{E_b}\right) \\ &\quad - \exp\left(-\frac{\hbar E_b + 2ak_B T\sqrt{2mE_b}}{\hbar k_B T}\right)\end{aligned} \tag{5}$$

from which an approximate solution for $\Pi_{\text{error}} = 0.5$ is

$$E_b^{\min} \approx k_B T \ln 2 + \frac{\hbar^2 (\ln 2)^2}{8ma^2}. \tag{6}$$

Solution of (6) gives a generalized value for minimum energy per switch operation at the limits of distinguishability that takes into account both classic and quantum transport phenomena. The plot given in Fig. 2 shows the numerical solution of (5) and its approximate analytical solution given by (6) for $\Pi_{\text{error}} = 0.5$. It is clearly seen that for $a > 5$ nm, the expression $E_b = kTln2$ is a valid representation of minimum energy per switch operation, while for $a < 5$ nm, the minimum switching energy can be considerably larger.

In order to change the state of a switch, the particle in a well should be provided additional energy to transition over the barrier. Alternatively, work needs to be done to reduce the height or width of the barrier. If the process is irreversible, this energy is converted into heat. For a given value of E_{bit}, we can use (2) and (6) to develop data relating the energy barrier height and width (a), switching time (t_{min}), error probability (Π_{error}), and power density (P) as displayed in Table 1.

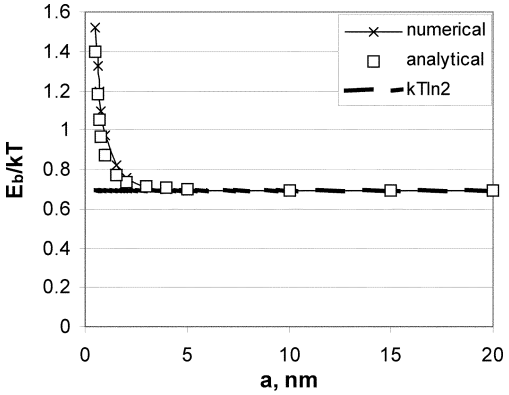

Fig. 2. Minimum energy per switch operation as a function of minimum switch size.

Table 1
Energy Barrier Height (E_b) and Width (a), Switching Time (t_{min}), Error Probability (Π_{error}), and Dense-Packed Circuit Power Density (P) of an "Ultimate Switch"

E_b (eV)	a (nm)	t_{min} (ps)	Π_{error} (%)	P (W/cm^2)
k_BTln2	1.5	0.04	56	$3.7\text{x}10^6$
k_BT	0.9	0.025	50	$1.1\text{x}10^7$
$10k_BT$	0.13	0.0025	50	$9.1\text{x}10^{10}$

Note that the SNL value for minimum switching energy $(E_{\text{SNL}} = k_B T ln2)$ underestimates the minimum switching energy required to operate the device. Due to tunneling, the error probabilities would always exceed 50% if the barrier height was set at $k_B Tln2$.

In fact, we can develop a device design constraint from the above arguments.

Suppose that there are n devices in a unit area A operating at a switching frequency f. Let $P_{\max}$ denote maximum thermal power that can be removed from the chip per unit area. Then

$$P_{\max} \approx nE_b f \geq \frac{nf}{A}\left[k_b T \ln 2 + \frac{(\ln 2)^2 \hbar^2}{8ma^2}\right] \tag{7}$$

and tradeoffs between a and f are implied by the physical limit on heat removal capability.

As can be seen from Table 1, even "least energy computation" at SNL limit results in extremely high heat generation. However, for practical purposes, E_b must be much larger than E_{SNL}. If not, there is high static standby power dissipation, and a very high rate of false bit occurrences generated by thermal fluctuations (the latter problem was recently analyzed in [12]).

III. Limits of Heat Removal

The energy density bound of 5–10 MW/cm^2 obtained in this paper by invoking the Heisenberg Principle and distin-

guishability concept (see Table 1) is an astronomic number. By comparison, the power density of a light bulb filament is about 100 W/cm^2, and the power density of the surface of the sun is roughly 6000 W/cm^2. Clearly, scaling for maximum component densities depends on the maximum rate at which thermal energy can be removed from a solid. It is recognized that heat can only be removed from systems at some finite rate [4]; however, quantitative estimates of fundamental limits for heat removal from a heterogeneous solid system at moderate temperature gradients to the ambient are difficult to obtain because there exist several different heat removal mechanisms and because of the complex geometry of a packaged chip. Although fundamental limit estimates for heat removal capacity are beyond the scope of the paper, we outline a few basic thermal considerations below.

Any heat removal process implies the presence of a reservoir with an infinite heat capacitance, i.e., $T_a = \text{const}$, in which all heat ultimately flows. We take $T_a = 300$ K.

Newton's Law of Cooling is another governing principle for heat removal, i.e.

$$Q = H(T_{\text{dev}} - T_a) \tag{8}$$

where T_{dev} is the device temperature during operation, and H is the heat transfer coefficient. Note that (8) indicates the rate of heat removal is directly proportional to the difference between the ambient and the device temperature and requires that $T_{\text{dev}} > T_a = 300$ K. The maximum temperature of silicon integrated circuits is estimated to be about 400 K (125 °C [6]); thus, 300 K $< T_{\text{dev}} <$ 400 K.

A. Heat Removal at $T_{\text{dev}} > T_a$

The coefficient H in (8) varies significantly depending upon the cooling method chosen. The maximum values of H are limited by material constants such as specific heat, thermal conductivity, viscosity, etc. Highest values of H for $T_{\text{dev}} <$ 400 K can be achieved by using liquid forced convection and phase change/boiling [7]. Additional increase of the heat removal rate can be achieved by creating extended surface area [7]. In [8], it was estimated that the ultimate limit for heat removal from silicon surface at $T_{\max} <$ 400 K is about 1000 W/cm^2 by convective cooling. A similar heat removal capacity was estimated for phase change [7] and thermoelectric cooling [9]. Experimentally, 790 W/cm^2 was demonstrated by forced water convection cooling of a uniformly heated Si substrate with embedded microchannels [8]. In information-processing systems the upper limit of heat removal is somewhat lower, due to concentration of heat sources in local areas of the system. If known cooling methods are employed, it appears that that heat removal capacity of *several hundred* W/cm^2 represents a practically achievable limit for a two-dimensional structure. Note that ITRS projects 93 W/cm^2 for the year 2016, and this number is in the "no known solution" category.

(A similar analysis can be offered for heat removal capacities for a three-dimensional solid system, where the theoretical heat removal rates can be as high as 10 kW/cm^2 [10]. However, this is offset by much higher volumetric heat generation by the electronic components.)

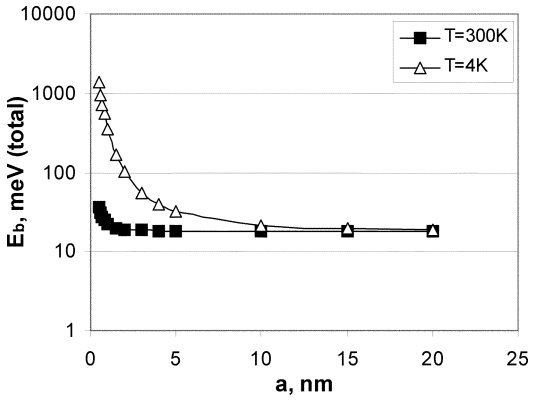

Fig. 3. The total energy per bit operation for room temperature and cryogenic operations of a nanoelectronic switch.

B. Heat Removal at $T_{\text{dev}} < T_a$

Another alternative is to remove the heat generated by the device by refrigeration. In this case, Carnot's Theorem gives the maximum efficiency for an ideal machine for forced heat removal

$$W_{\text{cool}} = \frac{T_a - T_{\text{device}}}{T_{\text{device}}} Q \tag{9}$$

where Q is the heat removed and W_{cool} is the work required to remove the heat. Since energy is consumed by refrigeration, one must consider the total energy consumed by both device operation and the refrigeration system

$$\begin{aligned} E_{\text{bit}}^{\text{total}} &= E_{\text{bit}} + \frac{T_a - T_{\text{dev}}}{T_{\text{dev}}} E_{\text{bit}} \\ &= \frac{T_a}{T_{\text{dev}}} E_{\text{bit}} \\ &= \frac{T_a}{T_{\text{dev}}} \left[k_B T_{\text{dev}} \ln 2 + \frac{\hbar^2 (\ln 2)^2}{8ma^2} \right] \\ &= k_B T_a \ln 2 + \frac{T_a}{T_{\text{dev}}} \frac{\hbar^2 (\ln 2)^2}{8ma^2}. \end{aligned} \tag{10}$$

Note from Fig. 3 that for nanodevice cryogenic operation, the total energy per bit increases dramatically relative to the total energy per bit required at room temperature. This increased dissipation is ultimately due to the temperature independence of the second term on the right side of (10) that arises from tunneling considerations.

IV. Reality Check: Comparison With the 2001 ITRS

Present day and projected silicon integrated circuits differ from the above model in several respects. First, the packing density is less than $1/a^2$, since the effective size of FET switch l is larger than the channel length a (in practice, $l = 10 - 15\ a$). Second, in integrated circuits, there exist many layers of interconnects that dissipate energy and also require some floorspace. It is well known that the minimum energy

Table 2
Comparison of the Results of This Analysis With Data Projected for CMOS Technology Projected for End-of-the-ITRS 22-nm Node MOSFETS for 2016 in the 2001 ITRS

Intergration density (transistors/cm^2)	This analysis ($n_{\max} = \frac{1}{x_{\min}^2}$)	4.7 x10^{13}
	2016 ITRS 22-nm Node (n_{2016})	2.9 x10^9
Switching Time (fs)	This Analysis ($t_{\min} = \frac{\hbar}{\Delta E}$)	40
	2016 ITRS 22-nm Node (t_{2016}=CV/I)	150
Power Density (W/cm^2)	This Analysis ($P_{\max} = \frac{n_{\max} kT \ln 2}{t_{\min}}$)	3.7x10^6
	2016 ITRS 22-nm Node	93
Normalized[1] Power Density(W/cm^2)	($P_{2016} = P_{\max} \times \frac{n_{2016}}{n_{\max}} \times \frac{t_{\min}}{t_{2016}}$)	61

[1]Normalized to the density and switching time of the ITRS projections for 2016 [6]

dissipated by interconnects for successful signal transmission is also $k_B T ln2/bit$. Therefore, taking into account that a part of chip area is occupied by interconnect does not substantially change estimate for minimum power.

Third, not all switches in the circuit change their state simultaneously; in other words, the activity factor is less than 100%.

Table 2 compares the results of the gedanken switch analysis with data projected for CMOS technology at the 2001 ITRS 22-nm node (2016) MOSFETs [5]. The table shows that if we scale the gedanken switch to a comparable density and speed to that of the end of the ITRS switch, the power dissipation per unit area is remarkably similar.

This comparison suggests two conclusions. First, any binary switch, operating at lower bound of energy, and in a maximum density configuration, fundamentally is limited in size to a critical dimension of $\sim$1 nm (see (2a) and Table 1). This critical dimension is less than 10$\times$ smaller than the critical dimension (9 nm) of an end-of-the-roadmap MOSFET.

Second, it is clear from the above analysis that scaling for binary switches, packed to maximum density, is ultimately limited by the system capability to remove heat. Even if we make an overoptimistic assumption that the devices operate at the SNL minimum energy limit, we can see than the benefits of scaling begin to erode as features' sizes approach those projected by the end of ITRS. This means that the simultaneous gains in packing density and speed of operation will eventually be replaced by a tradeoff between packing density and speed in order to satisfy heat removal constraints.

V. Summary and Implications

The 30-year-long trend in microelectronics has been to increase *both* speed *and* density by scaling of device components (e.g., CMOS switch). However, this trend will end as we approach the energy barrier due to limits of heat removal capacity. For nanoelectronics, this result implies that an increase in device density will require a sacrifice, due to power consideration, in operational speed, and vice versa. Thus, it appears that we are entering a regime where tradeoffs are required between speed and density, quite in contrast to the traditional simultaneous benefits in speed and density from conventional scaling.

Sometimes it is argued that enhanced processing speed at the algorithm level can be obtained via parallel execution, thus reducing the need for high-speed components. Indeed, in some cases, parallel execution can result in faster execution of a particular algorithm applied to a particular problem. In these cases, speedup in algorithm performance often is proportional to the number of additional elements utilized. Further, these additional computational elements usually are exercised at their limits of performance with high rate of component utilization. Consequently, the same fundamental limits on device size and speed, discussed above, remain operative.

We believe that in the next ten years, the impact of nanoelectronics research will be seen primarily through improvements in the evolution of the CMOS technology platform that will continue to advance along the lines prescribed by ITRS 2001. For example, new materials and processes are needed to reduce the gate and channel leakage problems associated with device scaling, and nonclassical MOSFET structures may be required to sustain scaling to and beyond the 22-nm technology node. Exotic structures, such as carbon nanotubes, may find their way into CMOS applications, not so much driven by acceleration of the scaling cadence, but more likely to enhance the performance of CMOS devices, or perhaps to simplify fabrication. The gedanken model above suggests that even if entirely different electron transport devices are invented for digital logic, their scaling for density and performance may not go much beyond the ultimate limits obtainable with CMOS technology, due primarily to limits on heat removal capacity. We think that this suggests that research to extend the benefits of scaling beyond the ITRS horizon should examine alternate physical mechanisms for device operation. All forms of information processing technology would significantly benefit from advances in heat removal technology.

References

[1] C. Mead and L. Conway, Eds., *Introduction to VLSI Systems*. Reading, MA: Addison-Wesley, 1980.

[2] R. T. Bate, "Quantum-mechanical limitations on device performance," in *VLSI Electronics*, N. G. Einspruch, Ed. New York: Academic, 1982, vol. 5.

[3] R. W. Keyes, Ed., *The Physics of VLSI Systems*. Reading, MA: Addison-Wesley, 1987.

[4] R. W. Keyes, "Fundamental limits in physical information processing," *Proc. IEEE*, vol. 69, no. 2, pp. 267–268, 1981.
[5] A. P. French and E. F. Taylor, Eds., *An Introduction to Quantum Physics*. New York: Norton, 1978.
[6] Semiconductor Industry Association (SIA), *International Technology Roadmap for Semiconductors*, International SEMATECH, Austin, TX, 2001.
[7] I. Mudawar, "Assessment of high-heat-flux thermal management schemes," *IEEE Trans. Comp. Packag. Technol.*, vol. 24, pp. 122–141, June 2001.
[8] D. B. Tuckerman and R. F. W. Pease, "High-performance heat sinking for VLSI," *IEEE Electron Device Lett.*, vol. EDL-2, pp. 126–129, May 1981.
[9] C. LaBounty, A. Shakouri, and J. E. Bowers, "Design and characterization of thin film microcoolers," *J. Appl. Phys.*, vol. 89, no. 7, pp. 4059–4064, Apr. 2001.
[10] H. M. Ozaktas, H. Oksuzoglu, R. F. W. Pease, and J. W. Goodman, "Effect of heat removal requirements in three-dimensional systems," *Int. J. Electron.*, vol. 73, no. 6, pp. 1227–1232, 1992.
[11] K. K. Likharev, "Classical and quantum limitations on energy-consumption in computation," *Int. J. Theor. Phys.*, vol. 21, pp. 311–325, 1982.
[12] L. B. Kish, "End of Moore's law: thermal (noise) death of integration in micro and nano electronics," *Phys. Lett. A*, vol. 305, pp. 144–149, 2002.

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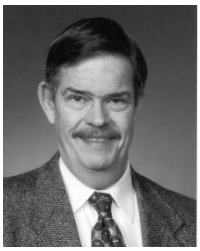

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