RAMBUS ROLLS OUT YELLOWSTONE

FlexPhase Circuit Design to Speed DRAMs and More

By Peter N. Glaskowsky {7/15/02-01}

Rambus has revealed the third major element of its Yellowstone signaling technology, which will be used in next-generation specialty memory devices for graphics cards, consumer electronics, and networking applications. The company's new FlexPhase circuit technology, which was demonstrated at the Rambus Developer Forum in Japan earlier this month, compensates for pin-to-pin timing skew problems, synchronizing multiple data lines to a single clock signal at higher data rates than would otherwise be possible. Skew is reduced to as little as 2.5ps by separate, programmable delay generators for the input and output paths on each pin of a Yellowstone memory controller.

FlexPhase is initially targeted to memory subsystems that approximate point-to-point configurations—just one or two memory devices attached to each data line. Figure 1 shows an example of a Yellowstone memory subsystem for a graphics card with one 64-bit DRAM bank. Each DRAM data pin is connected to one controller data pin. Two other buses that carry command and address information connect to two DRAMs each; these buses do not use FlexPhase.

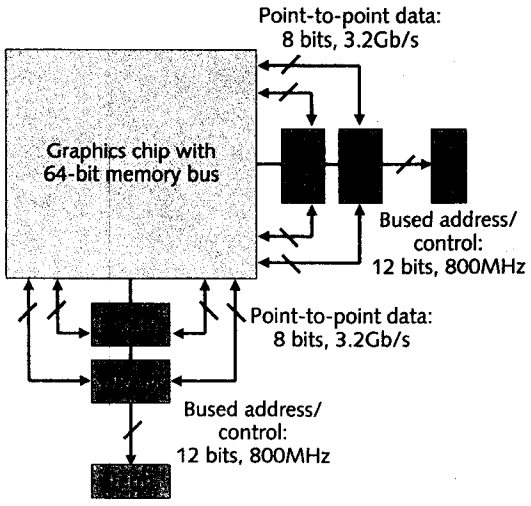

Figure 1. This example Yellowstone memory subsystem for a graphics card provides a 64-bit, 3.2Gb/s data interface to four 16-bit DRAMs. Two address/control buses each drive two of the DRAMs.

Other skew-reduction techniques, such as that included in the now-defunct SyncLink proposal (see *MPR 5/6/96-05*, "SDRAMs Ready to Enter PC Mainstream"), include retiming circuits in each device to support the large multidrop memory buses required in PC main-memory applications. FlexPhase removes these circuits from DRAMs, which are highly sensitive to manufacturing and testing costs, and supports bidirectional databuses instead of the unidirectional connections the SyncLink approach requires.

FlexPhase works with two previously announced elements of Yellowstone: the Differential Rambus Signaling Levels (DRSL) specification and octal data-rate (ODR) signaling. DRSL uses differential signal pairs with just 200mV of swing (from 1.0V to 1.2V) to reduce bus power and crosstalk to less than those of other low-voltage interfaces. ODR signaling involves distributing a 400MHz clock signal along with 3.2Gb/s data. Rambus says Yellowstone will scale up to 800MHz clock and 6.4Gb/s per-pin data rates, although the company has demonstrated only the 3.2Gb/s version of the interface.

FlexPhase Eases PCB Design

Minimizing skew at the Yellowstone controller allows data signals on printed-circuit boards (PCB) to be laid out without the serpentine tracks that have become common on motherboards and add-in cards. Each control/address bus still needs its traces matched in length, but each of these buses can be connected to as many as 18 DRAMs. Figure 2 shows the PCB routing for a configuration that has two chips per DRAM bank. These plots define the top and bottom layers of a four-layer board; the two inner layers are for power and ground, which carry no signal wiring.

FlexPhase provides 256 steps of adjustability across 625ps, or 2.5ps per step. This range is equivalent to two bit periods, but FlexPhase incorporates other techniques that let it compensate for delay mismatches amounting to several bit periods. The system can also tolerate impedance errors of ±15% resulting from PCB manufacturing variations.

The Yellowstone bus controller runs a FlexPhase calibration procedure when powered up. This procedure is expected to take less than 10ms and need not be repeated later. The calibrated delays center the data-sampling clock edges within a window that typically equals more than 50% of the 312ps bit time. Rambus says this figure includes transmitter, channel, and receiver timing errors and reflects the window size seen by the customer logic that is connected to the Yellowstone I/O receivers.

The FlexPhase circuitry adds some extra die area to the controller. A single I/O data byte occupies about 0.8mm^2 in a 0.13-micron process, including the PLL that receives the incoming 400MHz clock signal and distributes a multiplied-up 1.6GHz clock signal to each I/O bit. According to Rambus, this die-area penalty is similar to that required to implement the Rambus Access Controller (RAC) in previous RDRAM controllers. Unlike RDRAMs, however, Yellowstone-compatible memory devices do not require the same I/O circuitry that the controller does.

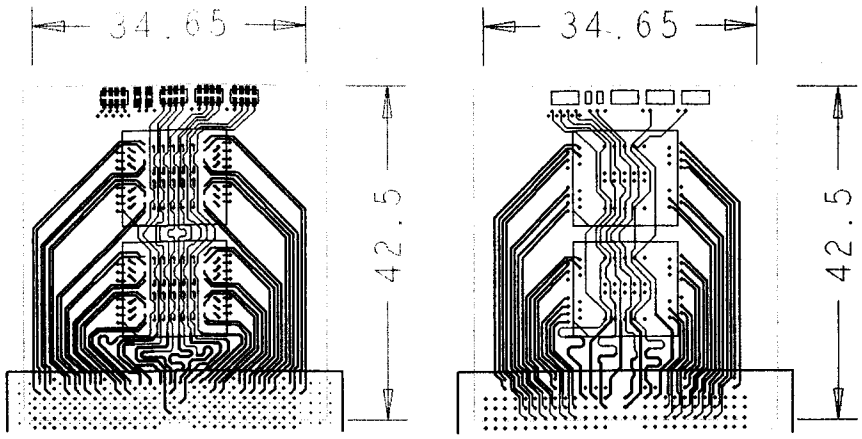

Figure 2. These plots show the top and bottom layers of a four-layer board equipped with two 16-bit DRAMs in chip-scale packages. The control/address bus through the center of the chips has length-matched traces, but FlexPhase makes it unnecessary to match the lengths of the 32 data pairs.

According to Rambus, Yellowstone solutions will scale up to about 100GB/s of total bandwidth within the pin counts and packaging technology used in today's graphics chips. A 128-bit Yellowstone implementation running at 6.4Gb/s will deliver that figure, meeting the needs of high-end PC graphics chips for several years to come. Rambus expects that customers will be able to implement a 128-bit controller on two sides of a 1,000-pin package. Although the number of data lines is doubled by Yellowstone's differential signaling, a corresponding reduction in the number of power and ground signals is needed to reduce power-supply impedance. Rambus believes the total number of pins for a Yellowstone interface will be similar to that needed for current high-speed single-ended DRAM interfaces.

Rambus is devoting its initial Yellowstone marketing efforts to applications in memory systems, but we believe the technology is appropriate for other chip-to-chip signaling uses. Yellowstone offers per-pin bandwidth similar to that of pure serial buses, such as PCI Express, without the 20% bandwidth reduction required by the 8B–10B clock encoding in that standard. An even greater advantage can be seen by comparing the die area that the FlexPhase circuitry requires to the silicon needed to perform parallel-to-serial conversion, packetizing, buffering, equalization, and clock recovery in a PCI Express implementation. Both ends of the PCI Express connection require the same circuitry, but one end of each Yellowstone link can be much less complicated than the other.

It is probably too late to change PCI Express, but we could eventually see Yellowstone-based versions of other high-speed buses, such as HyperTransport and RapidI/O. The new technology will also be of great interest to makers of game consoles and networking equipment, where the demand for performance is almost insatiable. We doubt Rambus can push Yellowstone into main-memory applications without a powerful patron—and Intel is unlikely to provide such patronage, as it did with RDRAM—but Yellowstone is likely to succeed in many other markets on its own merits. ◇