Optimizing MOS Transistor Mismatch

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***Abstract*— An investigation of MOS transistor mismatch is undertaken and a methodology is developed for optimizing mismatch without increasing layout area. Dramatic improvements of up to 300% in matching can be realized by selecting the optimum W/L ratio without changing the overall WL area product. The theoretical basis for the obtainable improvements is fully described and an expression is derived and verified by experiment to predict the W/L ratio which gives optimum matching.**

***Index Terms*—Mixed analog-digital integrated circuits, modeling, MOS devices, MOSFET's.**

I. Introduction

TRANSISTOR matching has become a topic of increasing interest in recent years. Research work has focused upon modeling the trend of matching with device layout area [2], [3], and very useful analytical models have been developed. The devices tested in support of the work had minimum feature sizes of 3 μm [3] and 1.6 μm [2]. The advent of submicrometer technologies has meant that mechanisms affecting mismatch which were not significant for larger devices have become more pronounced in the submicrometer regime.

When attempting to match transistors, circuit designers place devices adjacent to each other. This means that for a circuit designer, local mismatch sources [2] (geometry dependence of mismatch) are more significant than global mismatch sources [2] (spacing dependence of mismatch). This work will focus solely on the geometry dependence of mismatch arising from local mismatch sources. Existing research in the area of MOS transistor matching relates mismatch to an area term, i.e., mismatch $\sim 1/\sqrt{WL}$. The work presented here will show that DL and DW, the channel length and width reduction terms, have very significant contributions to the area when considered for mismatch. The expressions derived provide a method to predict these effects and indicate to the designer the relative strengths of each effect. Matching measurements were taken from a 0.8-μm CMOS process. The ability to improve matching and simultaneously reduce layout area has numerous applications within the field of electronic circuit design, including digital-to-analog converters [5], sense amplifiers for memory arrays [6], reference sources, etc.

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In this work, measurements of the mismatch in threshold voltage V_T, maximum transconductance β, and drain current were taken.

A. Test Structure

In order to assess the impact on mismatch of varying the (W/L) ratio without altering layout area, a test structure of devices with differing W and L ratios but with identical areas ($W.L$) was laid out. The structures contained adjacent pairs of devices with no special layout features. A large range of transistor geometries were available, $W/L = 1.66/6.66, 2.5/6.66, 8.33/6.66, 1.66/2, 1.66/1.33, 8.33/1.33, 1.66/0.8, 2.5/0.8, 8.33/0.8, 5/1.33, 1.66/4$ for NMOS, while for PMOS the same geometries were available with the exception that the minimum drawn channel length was 0.9 μm.

B. Threshold Voltage Mismatch

The work done here concerns the analysis of equal area devices with differing aspect ratios. The relationship shown in (1) below was derived separately in [2] and [3]. The expression predicts the mismatch for adjacent devices with equal layout areas

$$\sigma(\Delta V_T) = \frac{A_{VT0}}{\sqrt{WL}} \tag{1}$$

where A_{VT0} is a constant. Effective dimensions are defined as follows [10]:

$$W_{\text{eff}} = W_{\text{drawn}} - DW \tag{2}$$
$$L_{\text{eff}} = L_{\text{drawn}} - DL \tag{3}$$

where DL and DW are the channel length and width reduction parameters. DL is caused by lateral diffusion of the source and drain diffusions, while DW arises from encroachment of the field oxide into the channel. Fig. 1 shows the effective and drawn widths and lengths for two equal drawn area devices, an NMOS $W/L = 8.33/0.8$ device and a $W/L = 1.66/4$ device. Both devices have a layout area of 6.66 μm^2. The shaded area is the effective area for V_T mismatch. The figure illustrates how the geometry of the $W/L = 8.33/0.8$ device severely reduces its effective layout area $A_{\text{eff}} = 3.1$ μm^2, while the $W/L = 1.66/4$ device is affected to a much lesser degree $A_{\text{eff}} = 4.98$ μm^2. This effective layout area is strongly correlated to threshold voltage mismatch since other work has shown that substrate charge has a strong effect on V_T mismatch [3], [7] through the depletion charge term Q_B term in (4) below

$$V_T = V_{FB} + 2|\phi_B| + \frac{Q_B}{C_{OX}}. \tag{4}$$

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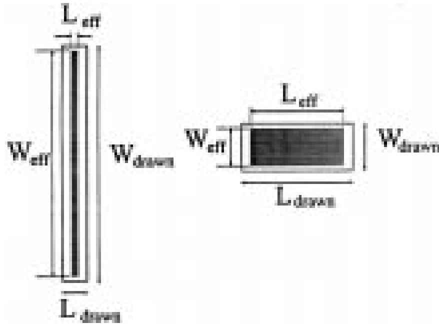

Fig. 1. Effective and drawn channel width and length for a $W/L = 8.33/0.8$ and $W/L = 1.66/4$ device. The layout area of both devices is 6.66 μm^2. The effective area for V_T mismatch is shaded. The short channel device has much smaller effective area than the narrow channel device.

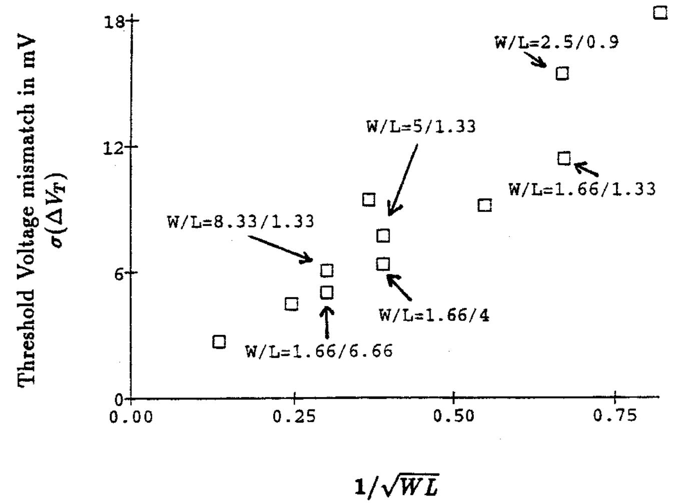

Fig. 2. V_T mismatch measurements for PMOS devices from a 0.8-μm process. Mismatch is plotted against $1/\sqrt{WL}$ where W and L are the drawn dimensions. The equal area devices are labeled. For equal layout area devices, shorter channel lengths and wider channel widths show poorer matching than longer channel lengths and narrower channel widths.

Equation (1) is restated below with the difference that the effective dimensions for V_T mismatch are now used instead of drawn dimensions

$$\sigma(\Delta V_T) = \frac{A_{VT0}}{\sqrt{W_{\text{eff}} L_{\text{eff}}}}. \tag{5}$$

In accordance with (5), transistors with larger effective areas will have better matching, i.e., smaller predicted $\sigma(\Delta V_T)$. This is confirmed by measurements. V_T mismatch measurements for PMOS devices are shown in Fig. 2 plotted against $1/\sqrt{WL}$ (where W and L have their drawn dimensions), the equal area devices have been labeled. If the equal area devices in Fig. 2 are examined, the following observations can be made.

- For equal drawn layout area devices, those with greater effective areas have better mismatch in accordance with (5).
- For equal drawn layout area devices, as channel length becomes shorter and channel width is relatively wide (large W/L), the effective layout area is greatly reduced and the matching is poor as predicted by (5).
- For equal drawn area devices, if channel length is relatively long, and width is narrow (small W/L), the effective area is larger and matching is better.

In Fig. 2, mismatch is plotted against $1/\sqrt{W_{\text{drawn}} L_{\text{drawn}}}$ and the graph is clearly not linear. If, however, the data from Fig. 2 is plotted against $1/\sqrt{W_{\text{eff}} L_{\text{eff}}}$ as shown in Fig. 3, a linear relationship exists as predicted by (5). This suggests that the effective dimensions which have been calculated are accurate and representative of the true effective areas for V_T mismatch. The results obtained so far suggest that a further step may be taken, and a general device may be optimized for matching purposes. If the effective area $W_{\text{eff}}.L_{\text{eff}}$ is maximized, it follows from (5) that the mismatch is minimized. The layout area is maximized by differentiating with respect to W_{eff} or L_{eff}, setting the expression equal to zero and solving

$$\begin{aligned} A_{\text{eff}} &= W_{\text{eff}} L_{\text{eff}} \\ A_{\text{eff}} &= (W_{\text{drawn}} - DW)(L_{\text{drawn}} - DL) \end{aligned} \tag{6}$$

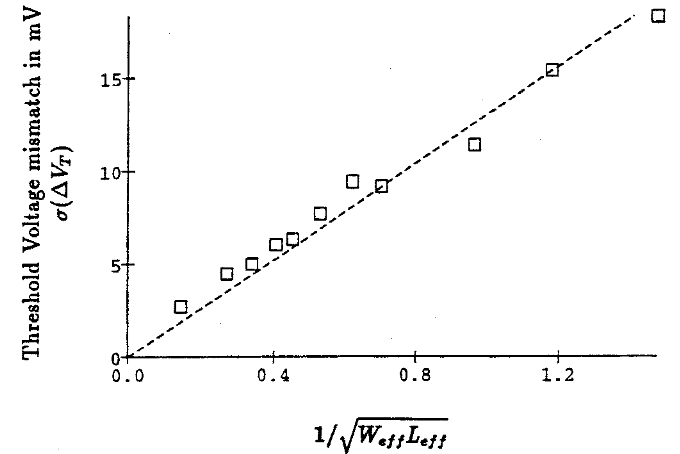

Fig. 3. V_T mismatch measurements for PMOS devices from a 0.8-μm process. Mismatch is plotted against $1/\sqrt{W_{\text{eff}} L_{\text{eff}}}$ where W_{eff} and L_{eff} are the effective dimensions for V_T mismatch as shown in Fig. 1. A linear relationship is apparent.

$$\frac{\delta(A_{\text{eff}})}{\delta(L_{\text{drawn}})} = \frac{A_{\text{drawn}}(DL)}{L_{\text{drawn}}^2} - DW = 0 \Rightarrow \frac{W_{\text{drawn}}}{L_{\text{drawn}}} = \frac{DW}{DL}. \tag{7}$$

Equation (7) is the drawn W/L ratio which will give optimum matching for any given layout area. The expression is independent of the drawn dimensions and has only process parameters as its arguments. The optimum drawn W/L ratios predicted using (7) for NMOS and PMOS from the 0.8-μm process tested were $W/L = 0.67$ and $W/L = 0.41$, respectively.

The relationship between threshold voltage mismatch and drawn (W/L) may be derived as follows. Equation (5) is restated

$$\begin{aligned} \sigma(V_T) &= \frac{A_{VT0}}{\sqrt{W_{\text{eff}} L_{\text{eff}}}} \\ \sigma(\Delta V_T) &= \frac{A_{VT0}}{\sqrt{(W_{\text{drawn}} - DW)(L_{\text{drawn}} - DL)}} \end{aligned} \tag{8}$$

$$\sigma(\Delta V_T) = \frac{A_{VT0}/L_{\text{drawn}}}{\sqrt{\left(\frac{W_{\text{drawn}}}{L_{\text{drawn}}} - \frac{DW}{L_{\text{drawn}}}\right)\left(1 - \frac{DL}{L_{\text{drawn}}}\right)}}. \quad (9)$$

Using (9), V_T mismatch versus drawn (W/L) may be predicted using process parameters and a value for A_{VT0} (slope of the fitted line) obtained from Fig. 3. The predicted and measured PMOS V_T mismatch versus (W/L) is shown in Fig. 4. A clear increasing trend of mismatch with (W/L) ratio is apparent from Fig. 4 for equal area devices. The figure shows good agreement between measured mismatch and mismatch predicted using the effective layout area dimensions.

C. β Mismatch

β is a combination of other parameters

$$\beta = \mu C_{OX} \frac{W_{\text{eff}}}{L_{\text{eff}}} \quad (10)$$

where μ is the channel mobility and C_{OX} is the gate oxide capacitance. Some variation in mobility μ will exist for different geometry devices, however, gate oxide capacitance will be virtually constant for adjacent devices. Research suggests that mobility variations are likely to be the dominant source of β parameter mismatch [2], [3]. By considering β as a function of four random variables [8] and following the derivation in [2] the following expression is obtained:

$$\frac{\sigma^2(\beta)}{\beta^2} = \frac{A^2_{W^2}}{W^2 L} + \frac{A^2_{L^2}}{L^2 W} + \frac{A^2_{\beta^2}}{WL} \quad (11)$$

where W and L refer to the drawn channel dimensions and A_W, A_L, A_β are constants. The effective dimensions arrived at for V_T mismatch no longer apply since they were derived with the assumption that substrate doping was the dominant source of mismatch, this cannot be assumed in the case of β mismatch. Before the advent of submicrometer technologies, the influence of the first two terms on the right hand side of (9) could be neglected because their influence was small when L or W was relatively large. However, when the drawn L is small as is the case here, the influence of these additional terms explains the difference in mismatch between equal area devices. For a short channel device, the term $A^2_{L^2}/L^2 W$ becomes significant and inflates the β mismatch. The term $A^2_{W^2}/W^2 L$ is not increased to the same extent for a narrow width device. Owing to the third term in (9), β mismatch will follow the same general trend as V_T mismatch (i.e., Mismatch $\sim 1/\sqrt{WL}$) except in the case of short channel devices which will tend to have inflated mismatch. Measured β mismatch for PMOS devices is shown in Fig. 5 plotted against $1/\sqrt{WL}$ (where W and L have their drawn dimensions). The equal area devices have been labeled on the graph. Fig. 5 shows that the difference in β mismatch for equal area devices is much greater than the corresponding difference in V_T mismatch for the same devices. The β mismatch data in Fig. 5 is consistent with the theoretical predictions described above, where devices with short channels show greater measured mismatch. If the β mismatch data in Fig. 5 is plotted against

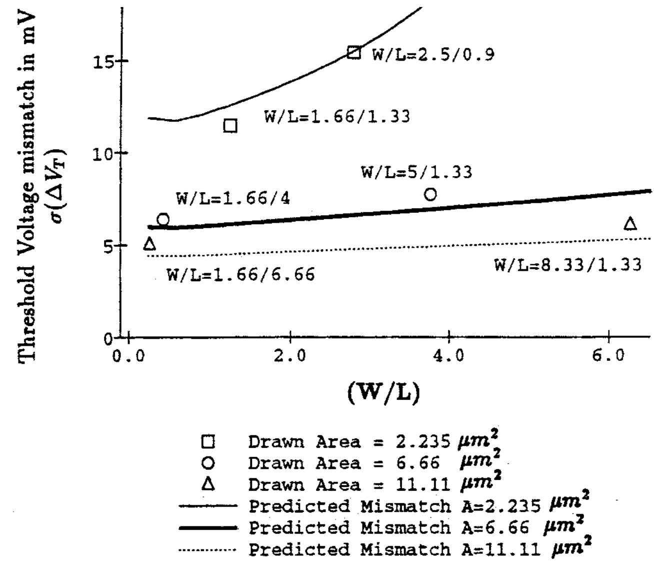

Fig. 4. Predicted and measured V_T mismatch for equal area PMOS devices from a 0.8-μm process. Mismatch is plotted against $1/\sqrt{WL}$. A clear increasing trend exists with W/L.

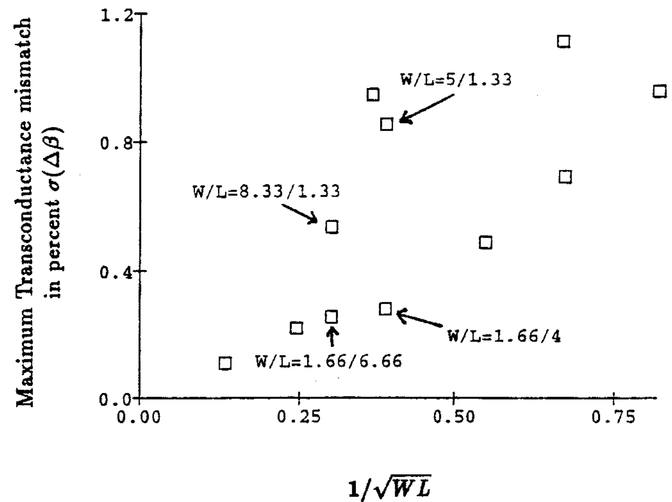

Fig. 5. β mismatch measurements for PMOS devices from a 0.8-μm process plotted against $1/\sqrt{WL}$ where W and L are the drawn dimensions. The equal area devices are labeled. For equal layout area devices, shorter channel lengths and wider channel widths show poorer matching than longer channel lengths and narrower channel widths.

drawn (W/L), a similar increasing linear trend is seen as was seen for V_T mismatch in Fig. 3.

It is apparent that in the case of β mismatch for equal drawn area devices, as was the case for V_T mismatch, a wide channel device with short channel length (large W/L ratio) has poorer matching than an equal area narrow channel transistor with relatively long channel length (small W/L ratio). This difference in matching can be as much as 300% (see Fig. 5).

D. Drain Current Mismatch

Drain current mismatch measurements were made on both NMOS and PMOS devices in the linear and saturation regions. The relationship between drain current mismatch and the

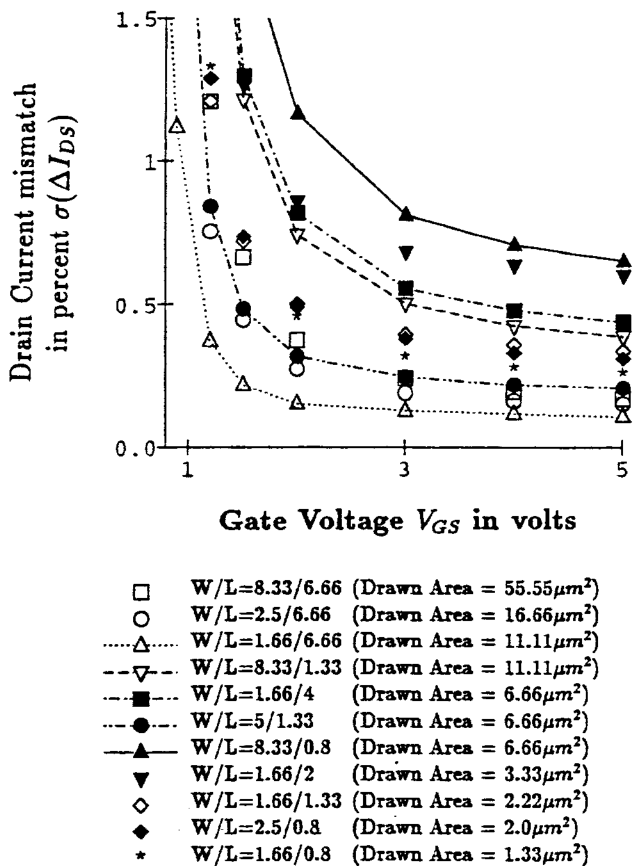

Fig. 6. Linear region drain current mismatch data for NMOS devices from a 0.8-μm process. The equal area devices have joined data points. For equal area devices, shorter channel lengths and wider channel widths show poorer matching than longer channel lengths and narrower channel widths.

mismatches in V_T and β was established in [3]

$$\frac{\sigma^2(\Delta I)}{I^2} = \frac{\sigma^2(\Delta\beta)}{\beta^2} + 4\,\frac{\sigma^2(\Delta V_T)}{(V_{GS} - V_T)^2}. \tag{12}$$

where $\sigma(\Delta V_T)$ and $\sigma(\Delta\beta)$ are the measured mismatches in V_T and β. The variations in mismatch between equal area devices which have been observed in V_T and β are transferred to I_{DS} mismatch through the relationship shown in (12) above. Fig. 6 shows measured linear region ($V_{DS} = 0.1$ V) drain current mismatch data taken from NMOS devices for a range of gate biases from threshold voltage up to +5 V. The equal area devices have connected data points. Below threshold (threshold voltage is approximately 0.8 V for NMOS on this process), mismatch reaches a maximum and levels out in the subthreshold region. The graphs show that I_{DS} mismatch improves steadily as gate bias increases in accordance with (12). A comparison between the I_{DS} matching performance of the equal area devices reveals that the same trends are present for drain current mismatch as were observed for V_T and β mismatch, namely that devices with a small W/L ratio have better matching than equal area transistors with a large W/L ratio. Drain current mismatch shows very dramatic improvements in matching for equal area devices of up to 500% obtained simply by selecting a smaller (W/L) ratio and without increasing layout area. It is also interesting to note that in Fig. 6, the device with the best matching performance is not the largest drawn area device, i.e., $W/L = 8.33/6.66$ ($A_{\text{eff}} = 55.55$), but rather the $W/L = 1.66/6.66$ ($A_{\text{eff}} = 11.11$) transistor has the best matching for all values of gate bias. By the same token, the device with the worst matching performance is not the smallest drawn layout area device, but the $W/L = 8.33/0.8$ ($W/L = 8.33/0.9$ for PMOS) transistor owing to the fact that it has minimum channel length and a large W/L ratio. Such observations are useful when considering matching issues for circuit design. Drain current mismatch data taken from the saturation region of operation ($V_{DS} = 5$ V) showed identical trends to those seen in Fig. 6. Likewise, I_{DS} mismatch data taken from PMOS devices showed similar trends to those observed for NMOS.

II. Conclusion

A test structure was designed to assess the influence of aspect ratio (W/L) on mismatch. The test structure incorporated many devices which had identical drawn layout areas but different aspect ratios. It was shown that for V_T, β, and I_{DS}, short channel lengths combined with wide channel widths (large W/L) degrade matching while relatively long channel lengths and narrow channel widths (small W/L) vastly improve matching. No mention has been made thus far of speed considerations. The work done here shows how longer channel lengths/narrow channel widths can improve mismatch. There exists a tradeoff with speed since longer channel lengths reduce speed. However, for certain critical analog circuit components such as sense amplifiers for memory arrays, this tradeoff is justified.

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