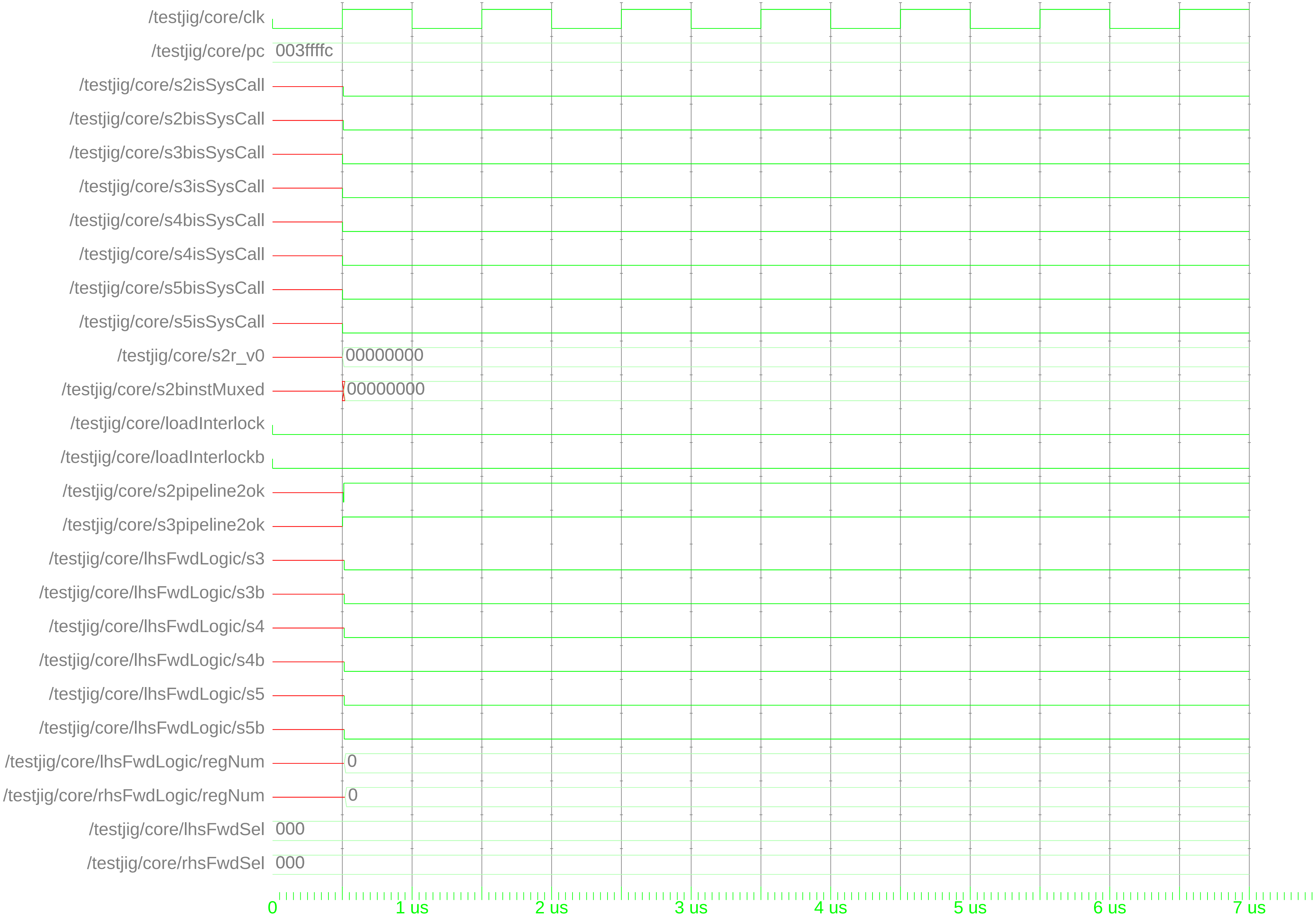
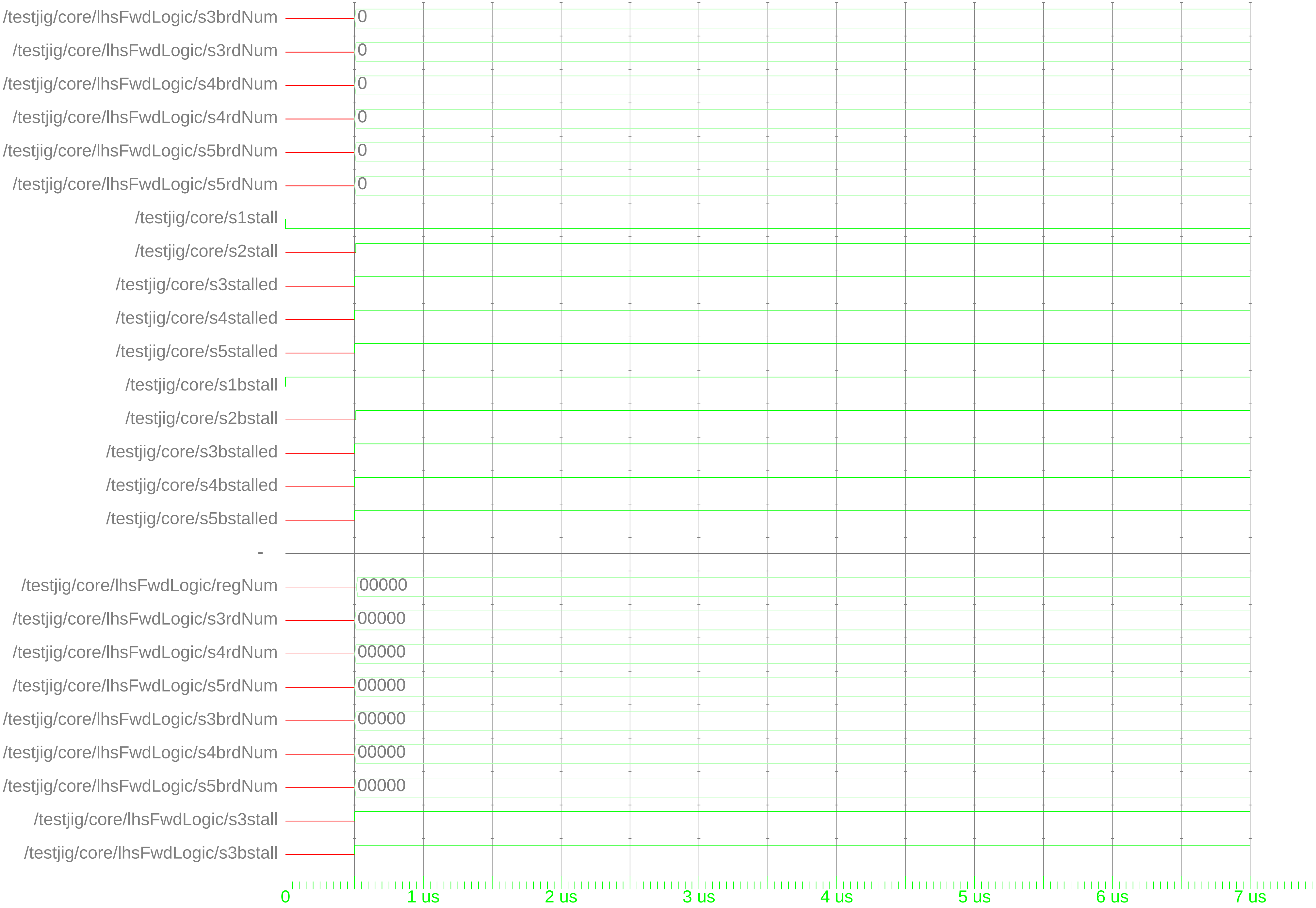
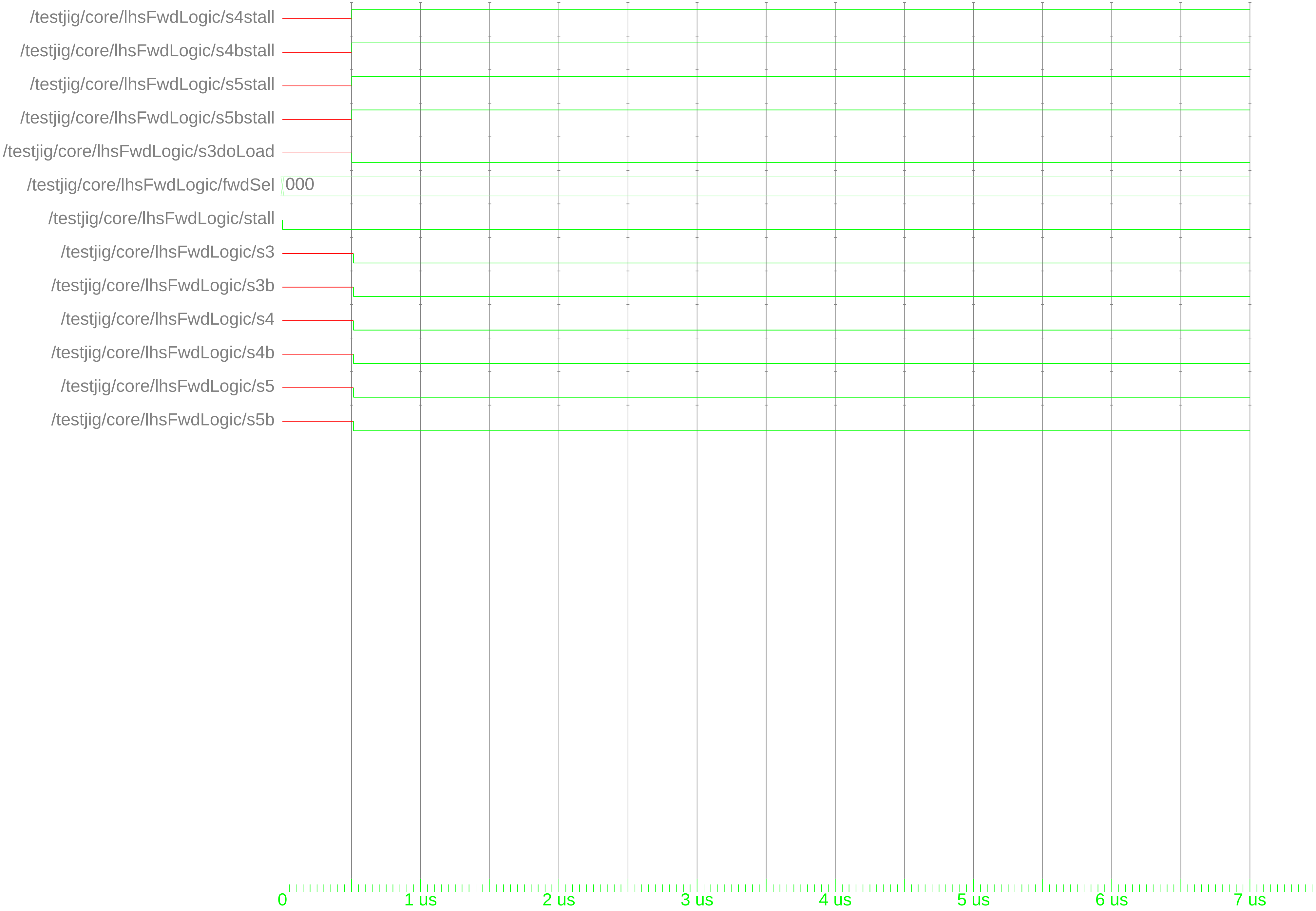
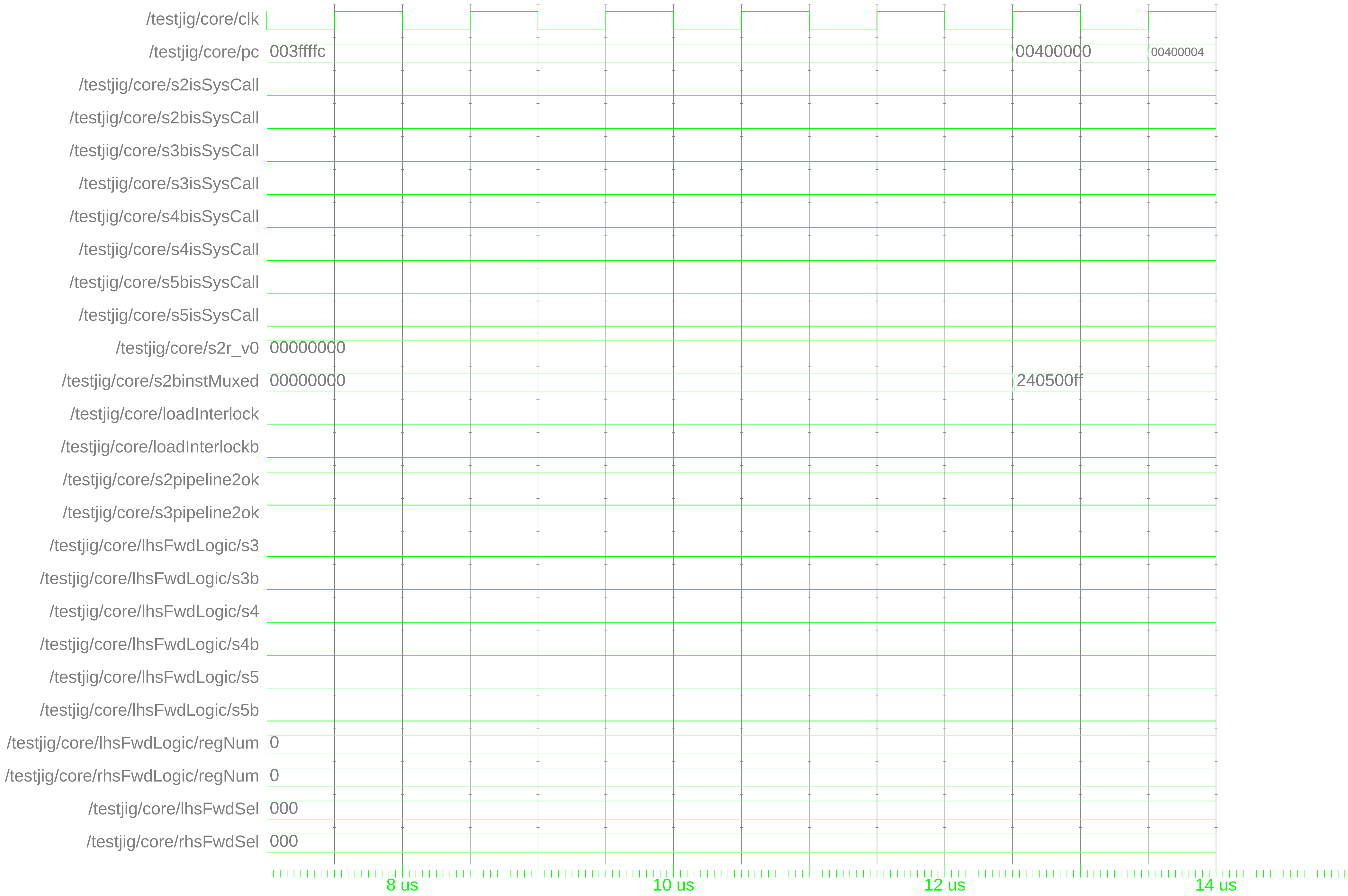


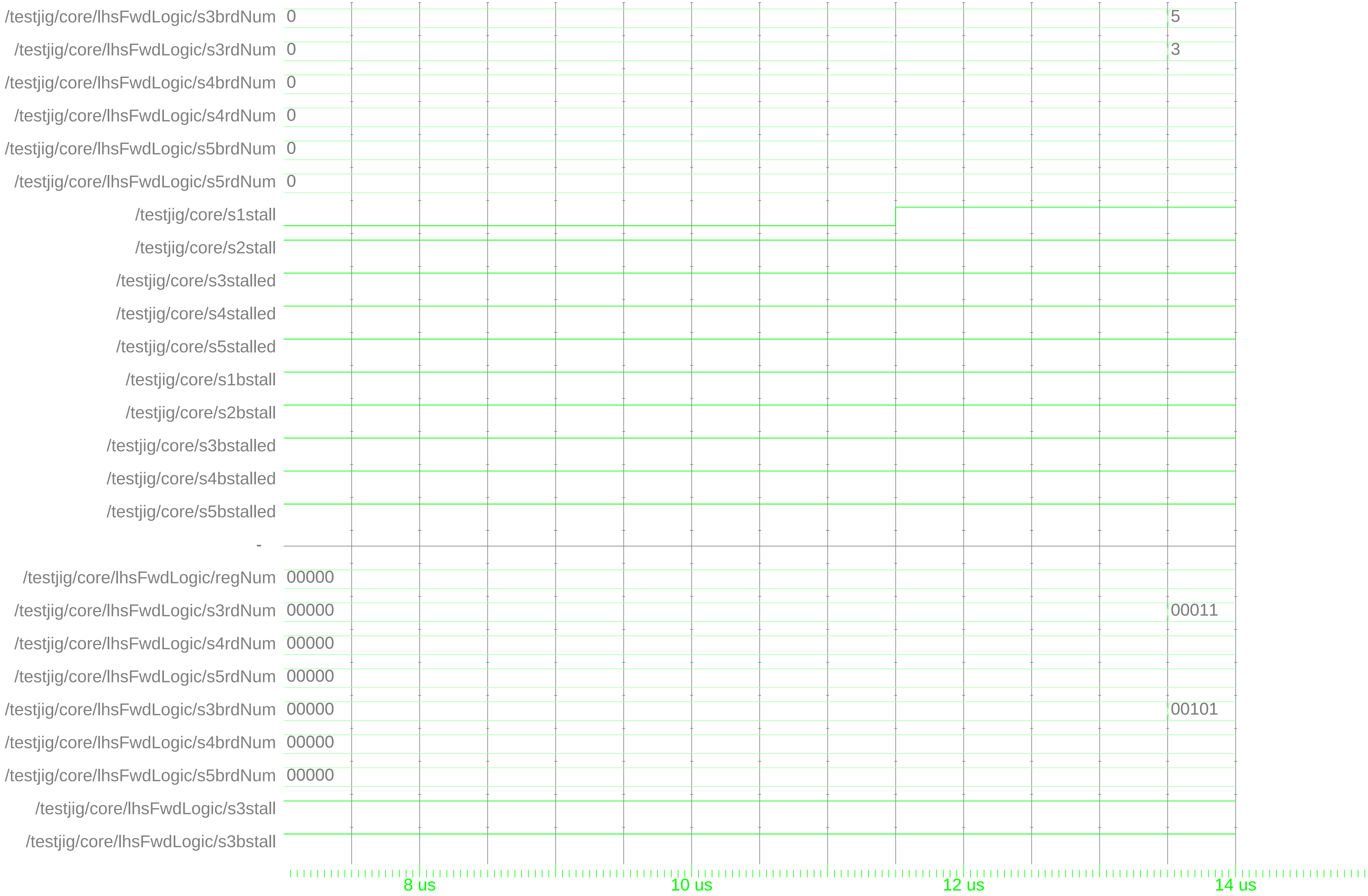
Entity:testjig Architecture: Date: Sat Dec 06 09:27:30 EST 2003 Row: 1 Page: 1

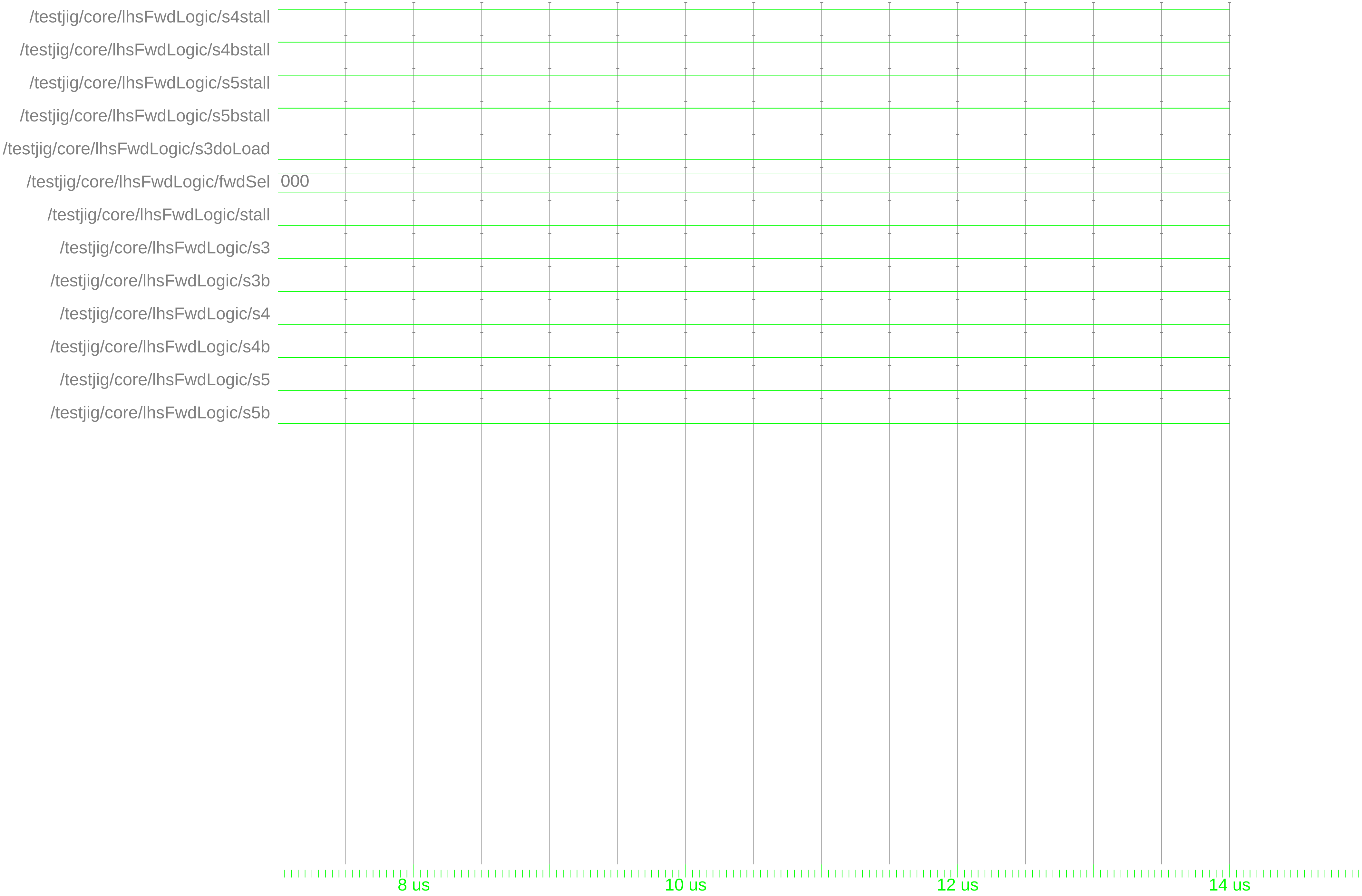


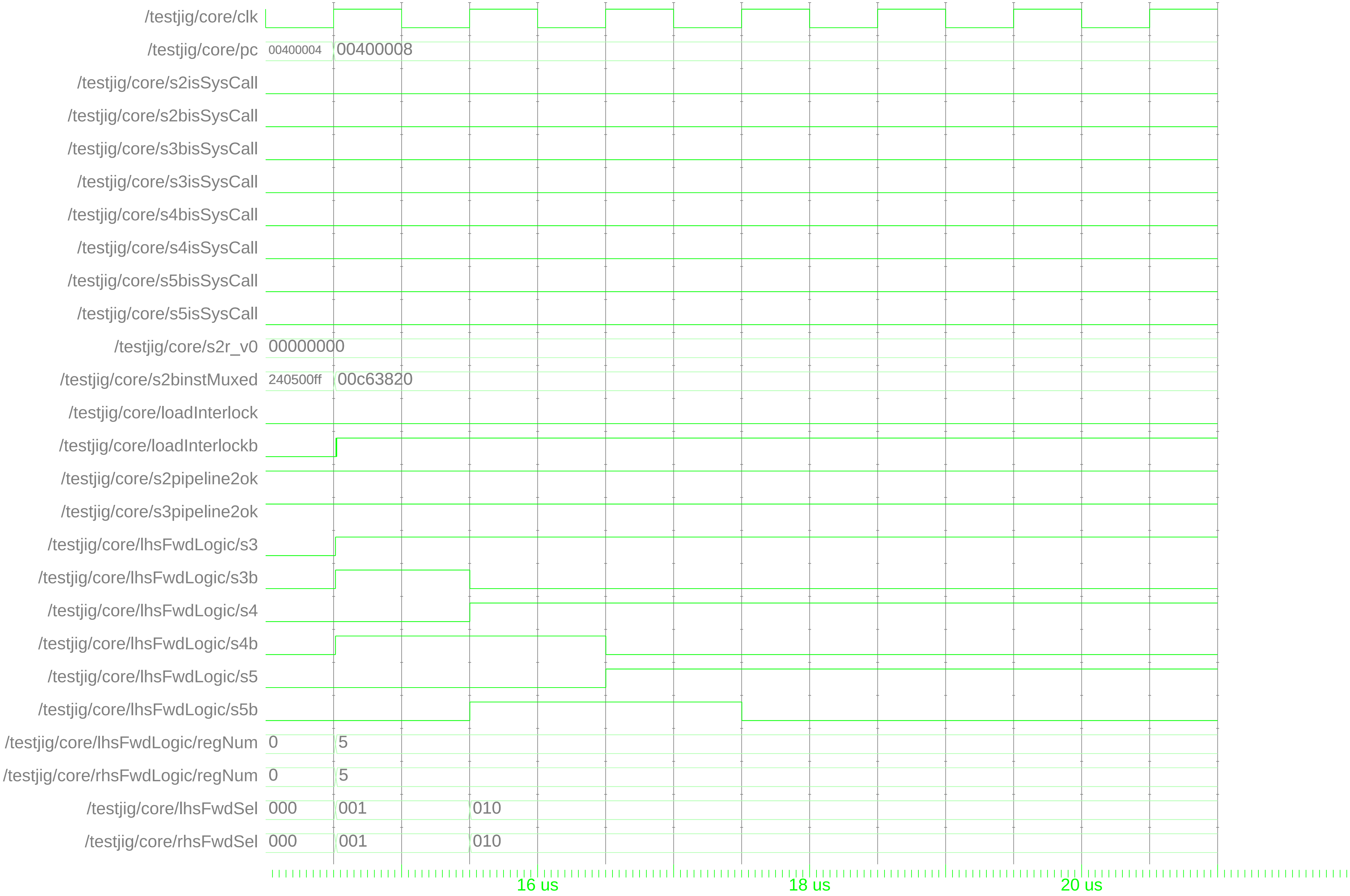
Entity:testjig Architecture: Date: Sat Dec 06 09:27:30 EST 2003 Row: 1 Page: 2

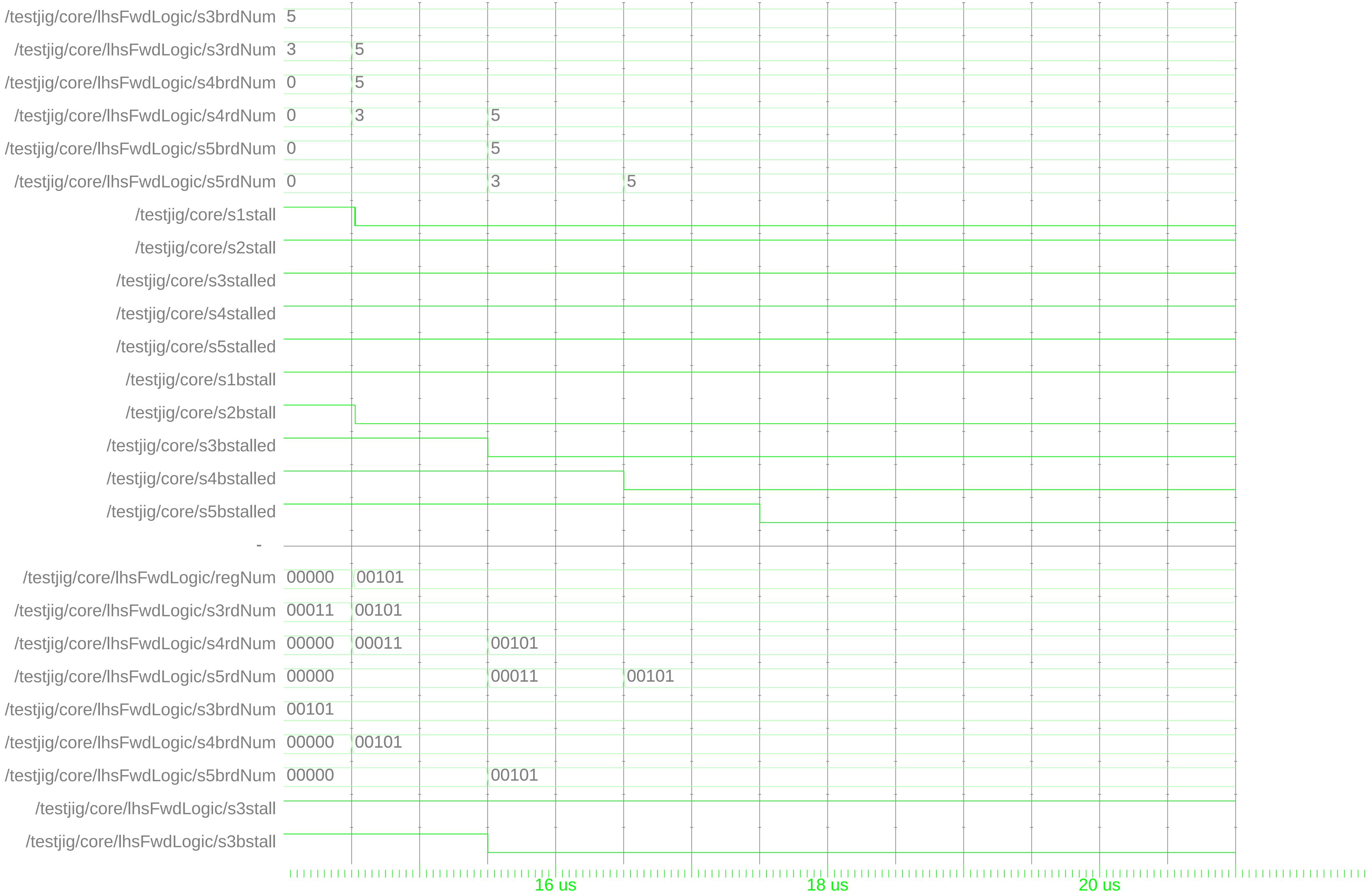

/testjig/core/lhsFwdLogic/s4stall
/testjig/core/lhsFwdLogic/s4bstall
/testjig/core/lhsFwdLogic/s5stall
/testjig/core/lhsFwdLogic/s5bstall
/testjig/core/lhsFwdLogic/s3doLoad
/testjig/core/lhsFwdLogic/fwdSel
000
/testjig/core/lhsFwdLogic/stall
/testjig/core/lhsFwdLogic/s3
/testjig/core/lhsFwdLogic/s3b
/testjig/core/lhsFwdLogic/s4
/testjig/core/lhsFwdLogic/s4b
/testjig/core/lhsFwdLogic/s5
/testjig/core/lhsFwdLogic/s5b
0
1 us
2 us
3 us
4 us
5 us
6 us
7 us

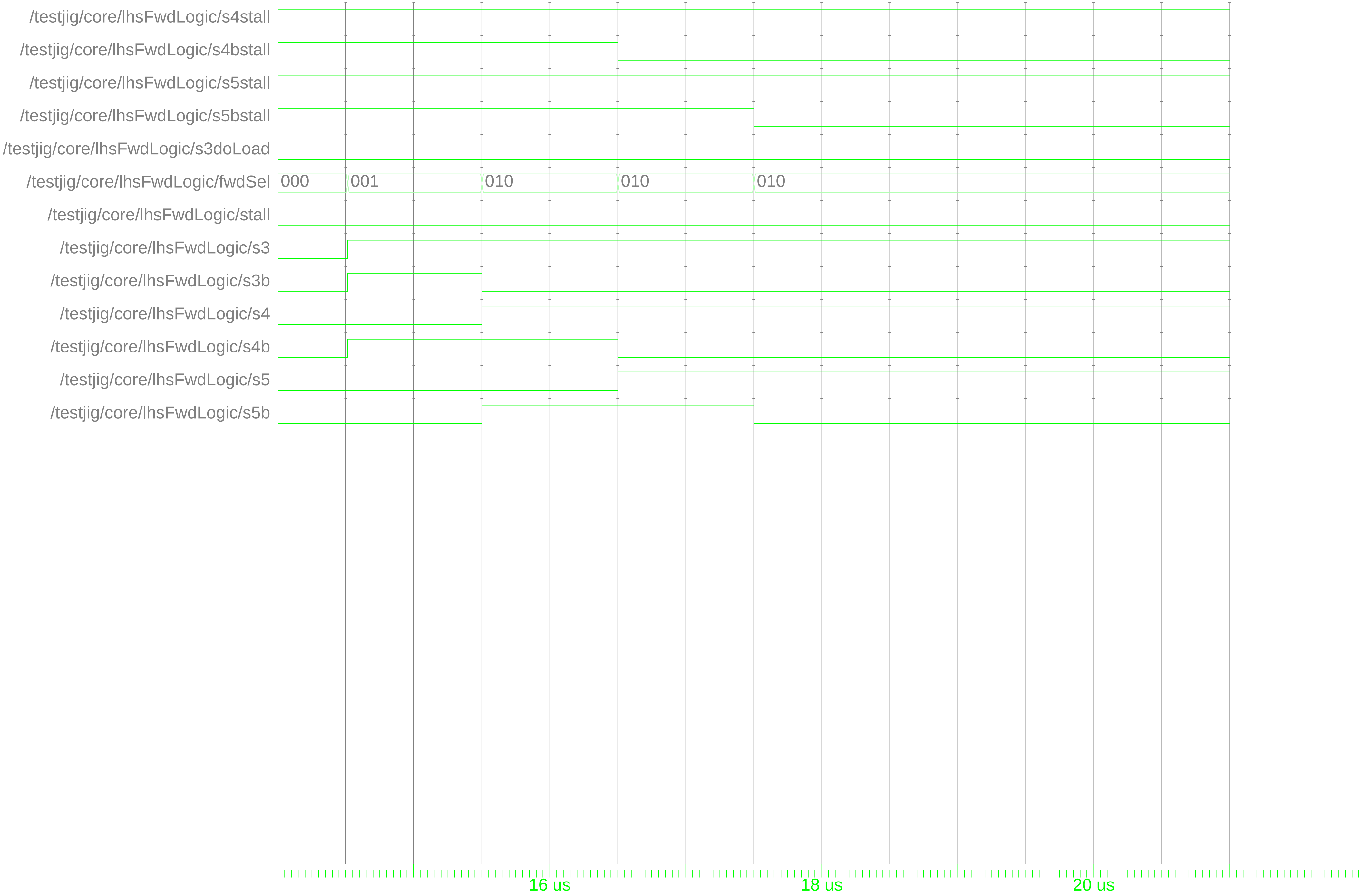

/testjig/core/clk
/testjig/core/pc
003ffffc
00400000
00400004
/testjig/core/s2isSysCall
/testjig/core/s2bisSysCall
/testjig/core/s3bisSysCall
/testjig/core/s3isSysCall
/testjig/core/s4bisSysCall
/testjig/core/s4isSysCall
/testjig/core/s5bisSysCall
/testjig/core/s5isSysCall
/testjig/core/s2r_v0
00000000
/testjig/core/s2binstMuxed
00000000
240500ff
/testjig/core/loadInterlock
/testjig/core/loadInterlockb
/testjig/core/s2pipeline2ok
/testjig/core/s3pipeline2ok
/testjig/core/lhsFwdLogic/s3
/testjig/core/lhsFwdLogic/s3b
/testjig/core/lhsFwdLogic/s4
/testjig/core/lhsFwdLogic/s4b
/testjig/core/lhsFwdLogic/s5
/testjig/core/lhsFwdLogic/s5b
/testjig/core/lhsFwdLogic/regNum
0
/testjig/core/rhsFwdLogic/regNum
0
/testjig/core/lhsFwdSel
000
/testjig/core/rhsFwdSel
000
8 us
10 us
12 us
14 us

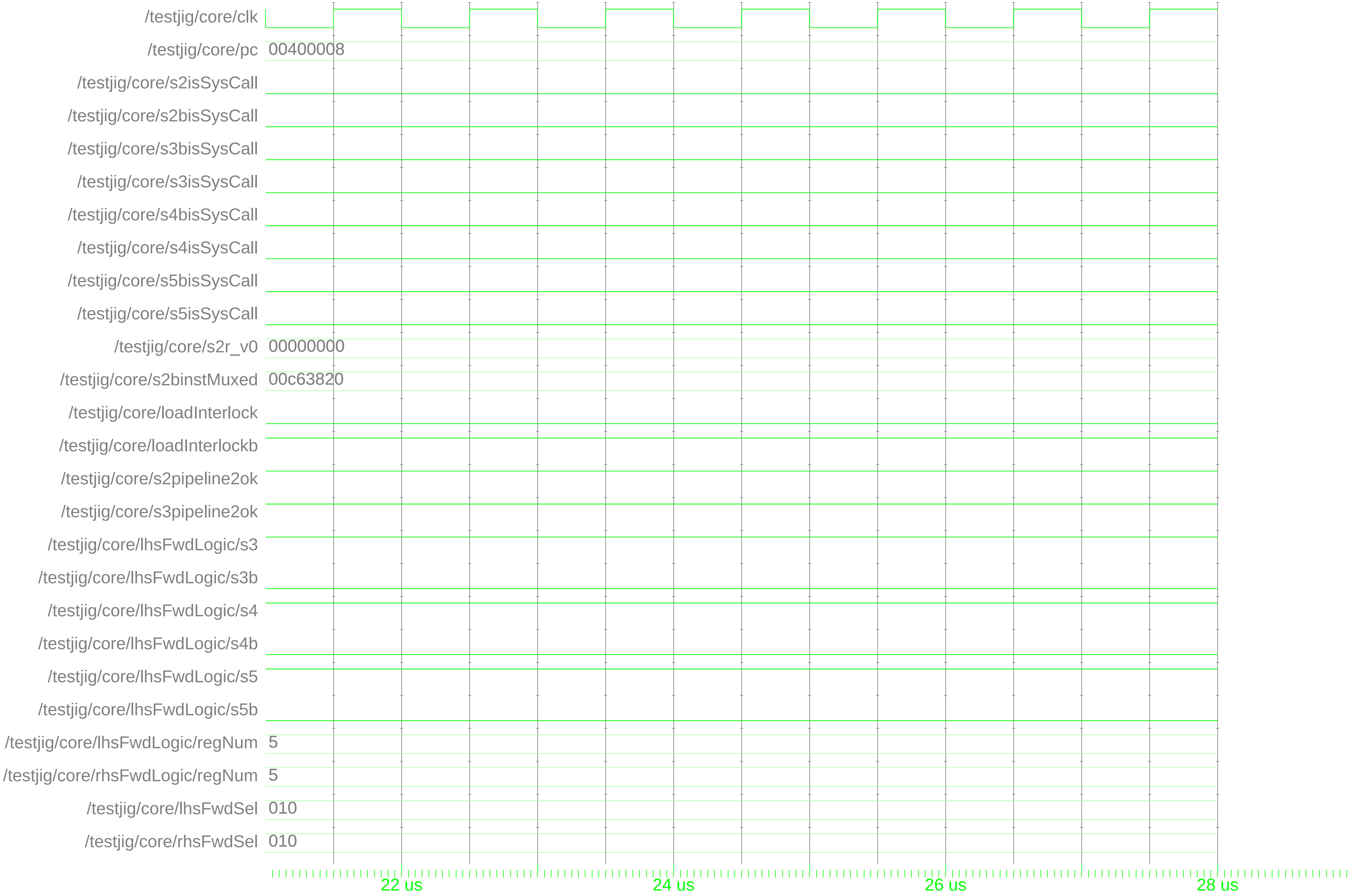

/testjig/core/lhsFwdLogic/s3brdNum
/testjig/core/lhsFwdLogic/s3rdNum
/testjig/core/lhsFwdLogic/s4brdNum
/testjig/core/lhsFwdLogic/s4rdNum
/testjig/core/lhsFwdLogic/s5brdNum
/testjig/core/lhsFwdLogic/s5rdNum
/testjig/core/s1stall
/testjig/core/s2stall
/testjig/core/s3stalled
/testjig/core/s4stalled
/testjig/core/s5stalled
/testjig/core/s1bstall
/testjig/core/s2bstall
/testjig/core/s3bstalled
/testjig/core/s4bstalled
/testjig/core/s5bstalled
-
/testjig/core/lhsFwdLogic/regNum
/testjig/core/lhsFwdLogic/s3rdNum
/testjig/core/lhsFwdLogic/s4rdNum
/testjig/core/lhsFwdLogic/s5rdNum
/testjig/core/lhsFwdLogic/s3brdNum
/testjig/core/lhsFwdLogic/s4brdNum
/testjig/core/lhsFwdLogic/s5brdNum
/testjig/core/lhsFwdLogic/s3stall
/testjig/core/lhsFwdLogic/s3bstall
0
5
0
3
0
0
0
0
00000
00000
00011
00000
00000
00000
00101
00000
00000
8 us
10 us
12 us
14 us

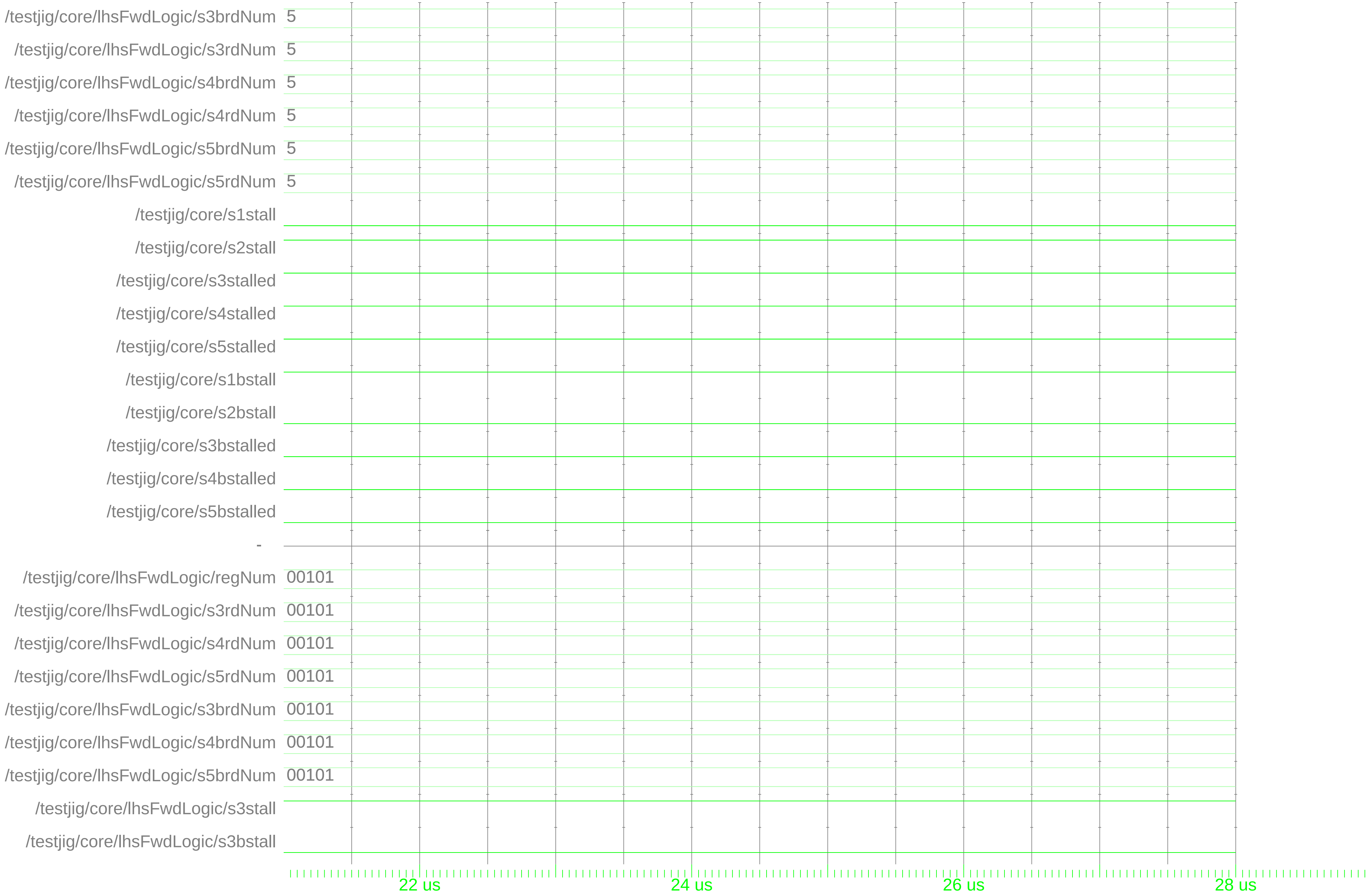

/testjig/core/lhsFwdLogic/s4stall
/testjig/core/lhsFwdLogic/s4bstall
/testjig/core/lhsFwdLogic/s5stall
/testjig/core/lhsFwdLogic/s5bstall
/testjig/core/lhsFwdLogic/s3doLoad
/testjig/core/lhsFwdLogic/fwdSel
000
/testjig/core/lhsFwdLogic/stall
/testjig/core/lhsFwdLogic/s3
/testjig/core/lhsFwdLogic/s3b
/testjig/core/lhsFwdLogic/s4
/testjig/core/lhsFwdLogic/s4b
/testjig/core/lhsFwdLogic/s5
/testjig/core/lhsFwdLogic/s5b
8 us
10 us
12 us
14 us

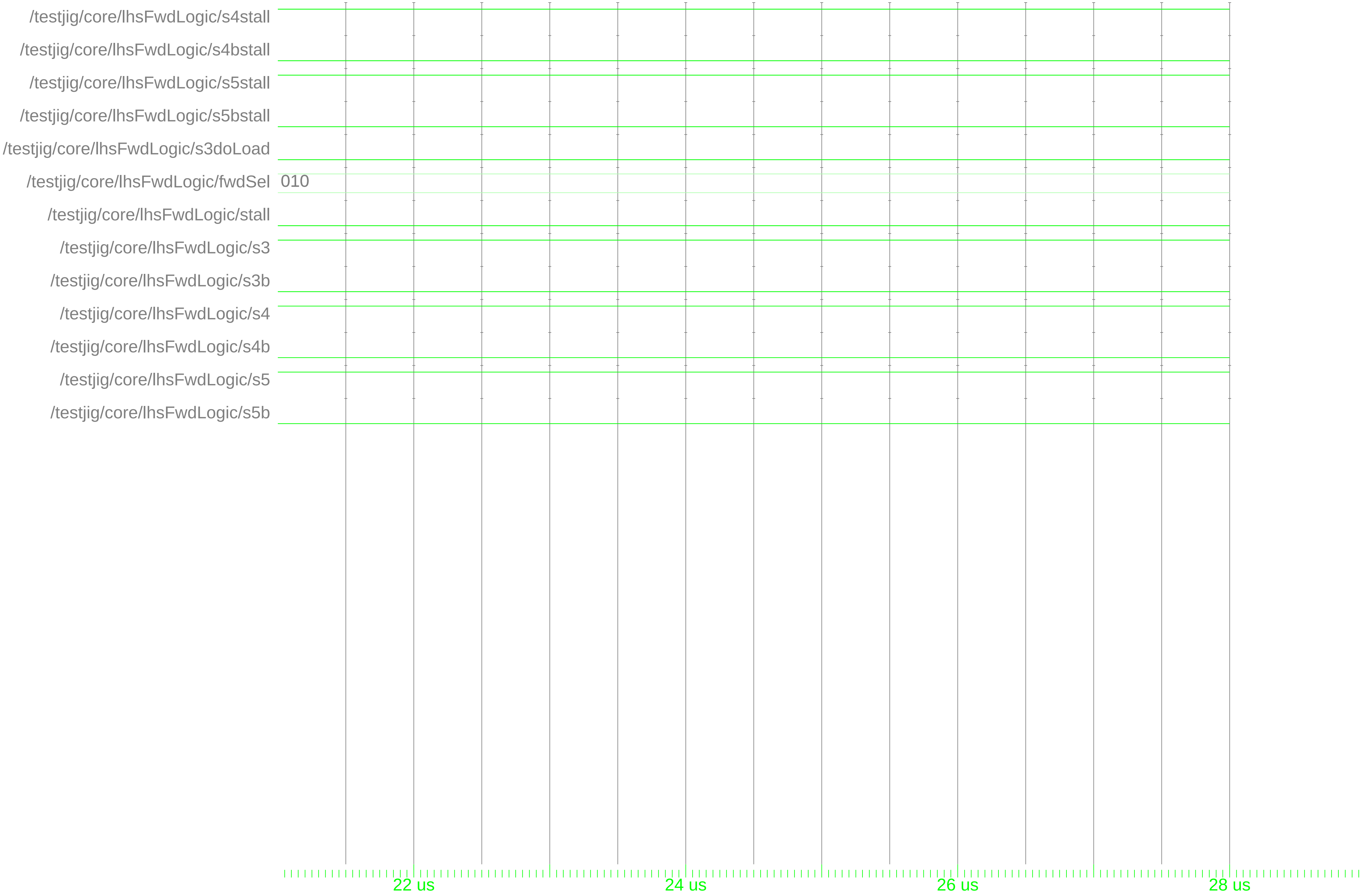

/testjig/core/clk
/testjig/core/pc
00400004
00400008
/testjig/core/s2isSysCall
/testjig/core/s2bisSysCall
/testjig/core/s3bisSysCall
/testjig/core/s3isSysCall
/testjig/core/s4bisSysCall
/testjig/core/s4isSysCall
/testjig/core/s5bisSysCall
/testjig/core/s5isSysCall
/testjig/core/s2r_v0
00000000
/testjig/core/s2binstMuxed
240500ff
00c63820
/testjig/core/loadInterlock
/testjig/core/loadInterlockb
/testjig/core/s2pipeline2ok
/testjig/core/s3pipeline2ok
/testjig/core/lhsFwdLogic/s3
/testjig/core/lhsFwdLogic/s3b
/testjig/core/lhsFwdLogic/s4
/testjig/core/lhsFwdLogic/s4b
/testjig/core/lhsFwdLogic/s5
/testjig/core/lhsFwdLogic/s5b
/testjig/core/lhsFwdLogic/regNum
0
5
/testjig/core/rhsFwdLogic/regNum
0
5
/testjig/core/lhsFwdSel
000
001
010
/testjig/core/rhsFwdSel
000
001
010
16 us
18 us
20 us

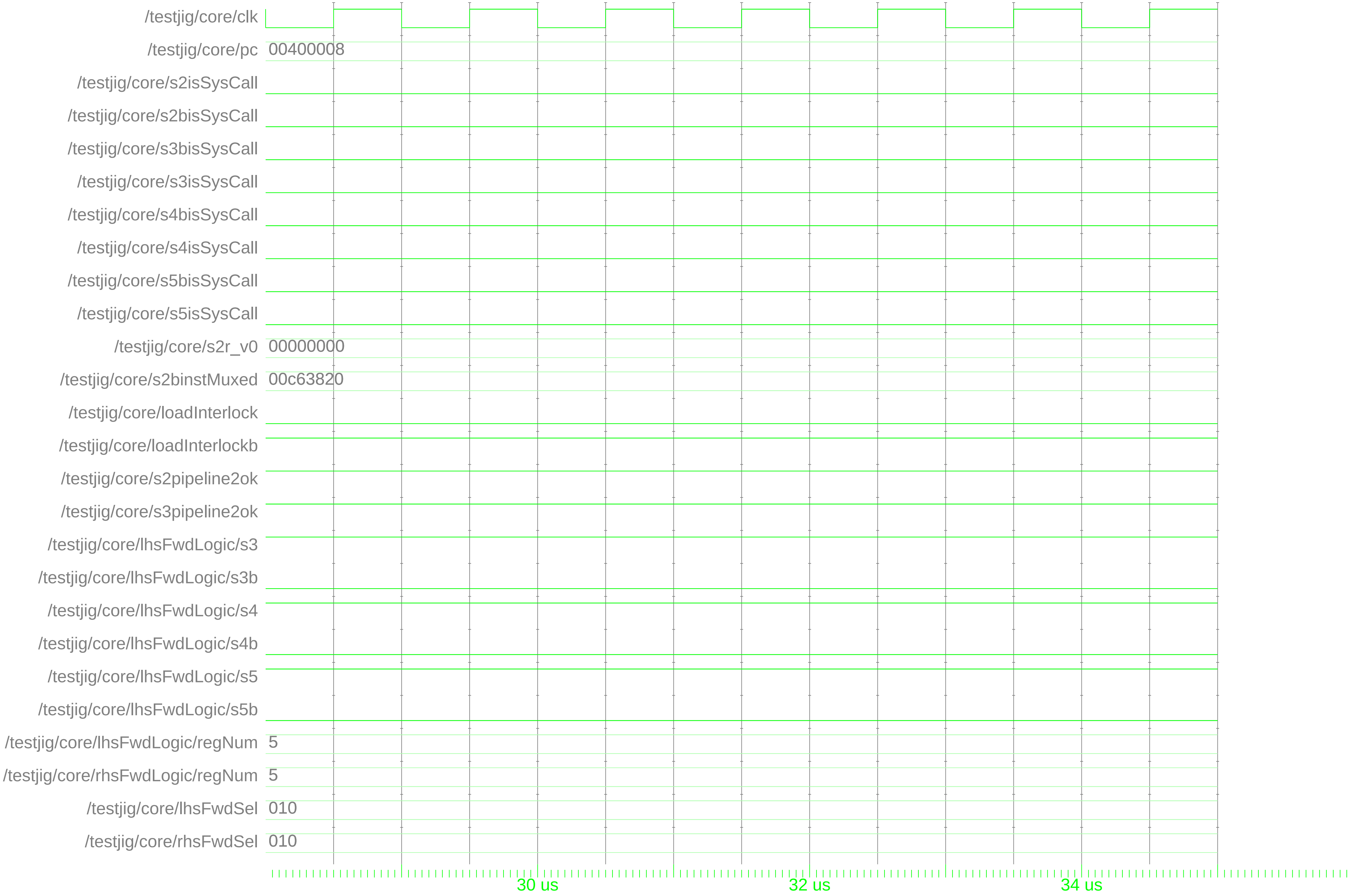

/testjig/core/lhsFwdLogic/s3brdNum 5
/testjig/core/lhsFwdLogic/s3rdNum 3 5
/testjig/core/lhsFwdLogic/s4brdNum 0 5
/testjig/core/lhsFwdLogic/s4rdNum 0 3 5
/testjig/core/lhsFwdLogic/s5brdNum 0 5
/testjig/core/lhsFwdLogic/s5rdNum 0 3 5
/testjig/core/s1stall
/testjig/core/s2stall
/testjig/core/s3stalled
/testjig/core/s4stalled
/testjig/core/s5stalled
/testjig/core/s1bstall
/testjig/core/s2bstall
/testjig/core/s3bstalled
/testjig/core/s4bstalled
/testjig/core/s5bstalled
-
/testjig/core/lhsFwdLogic/regNum 00000 00101
/testjig/core/lhsFwdLogic/s3rdNum 00011 00101
/testjig/core/lhsFwdLogic/s4rdNum 00000 00011 00101
/testjig/core/lhsFwdLogic/s5rdNum 00000 00011 00101
/testjig/core/lhsFwdLogic/s3brdNum 00101
/testjig/core/lhsFwdLogic/s4brdNum 00000 00101
/testjig/core/lhsFwdLogic/s5brdNum 00000 00101
/testjig/core/lhsFwdLogic/s3stall
/testjig/core/lhsFwdLogic/s3bstall
16 us
18 us
20 us


/testjig/core/lhsFwdLogic/s4stall
/testjig/core/lhsFwdLogic/s4bstall
/testjig/core/lhsFwdLogic/s5stall
/testjig/core/lhsFwdLogic/s5bstall
/testjig/core/lhsFwdLogic/s3doLoad
/testjig/core/lhsFwdLogic/fwdSel
/testjig/core/lhsFwdLogic/stall
/testjig/core/lhsFwdLogic/s3
/testjig/core/lhsFwdLogic/s3b
/testjig/core/lhsFwdLogic/s4
/testjig/core/lhsFwdLogic/s4b
/testjig/core/lhsFwdLogic/s5
/testjig/core/lhsFwdLogic/s5b
000
001
010
010
010
16 us
18 us
20 us

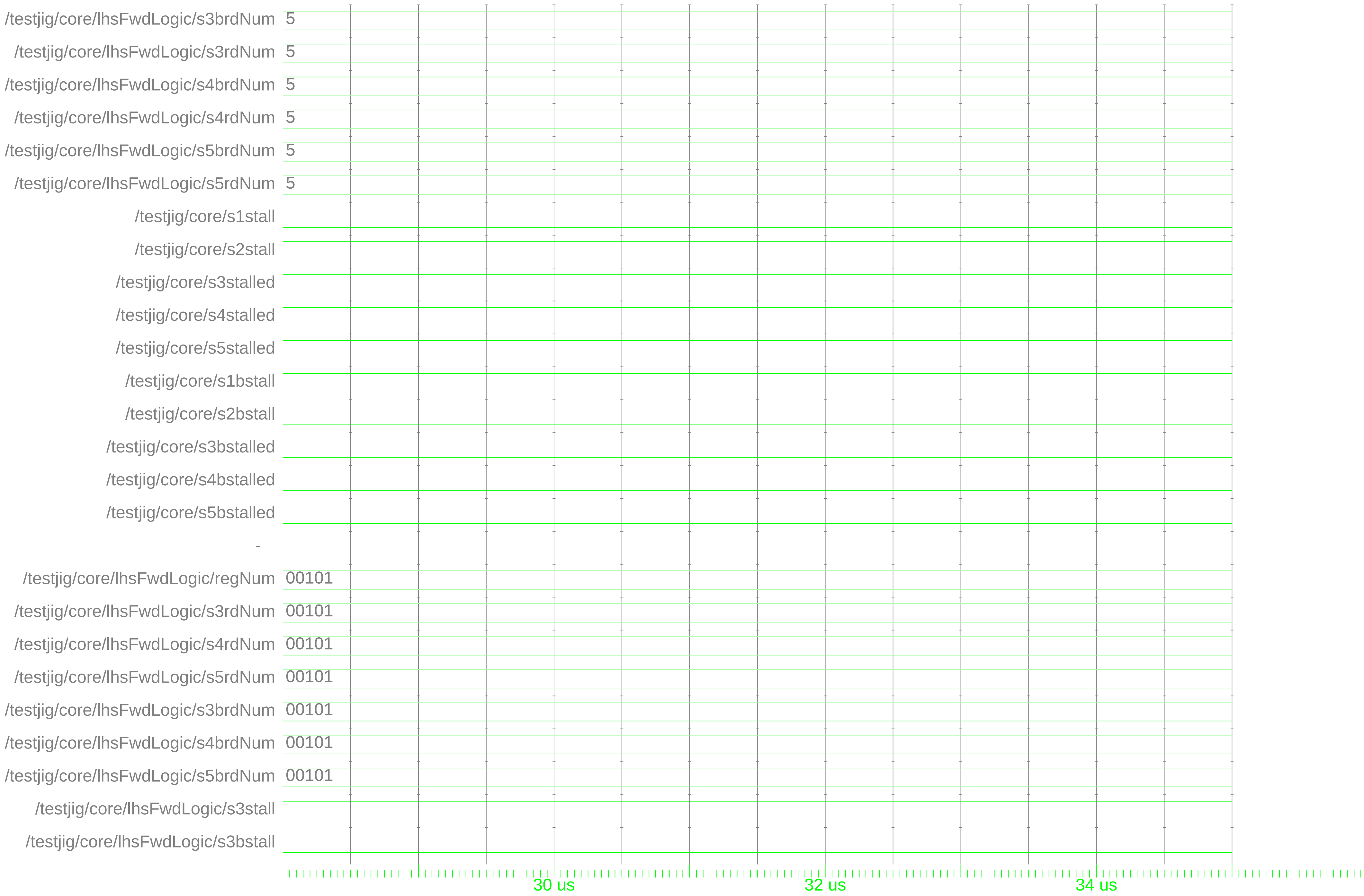

/testjig/core/clk
/testjig/core/pc 00400008
/testjig/core/s2isSysCall
/testjig/core/s2bisSysCall
/testjig/core/s3bisSysCall
/testjig/core/s3isSysCall
/testjig/core/s4bisSysCall
/testjig/core/s4isSysCall
/testjig/core/s5bisSysCall
/testjig/core/s5isSysCall
/testjig/core/s2r_v0 00000000
/testjig/core/s2binstMuxed 00c63820
/testjig/core/loadInterlock
/testjig/core/loadInterlockb
/testjig/core/s2pipeline2ok
/testjig/core/s3pipeline2ok
/testjig/core/lhsFwdLogic/s3
/testjig/core/lhsFwdLogic/s3b
/testjig/core/lhsFwdLogic/s4
/testjig/core/lhsFwdLogic/s4b
/testjig/core/lhsFwdLogic/s5
/testjig/core/lhsFwdLogic/s5b
/testjig/core/lhsFwdLogic/regNum 5
/testjig/core/rhsFwdLogic/regNum 5
/testjig/core/lhsFwdSel 010
/testjig/core/rhsFwdSel 010
22 us
24 us
26 us
28 us

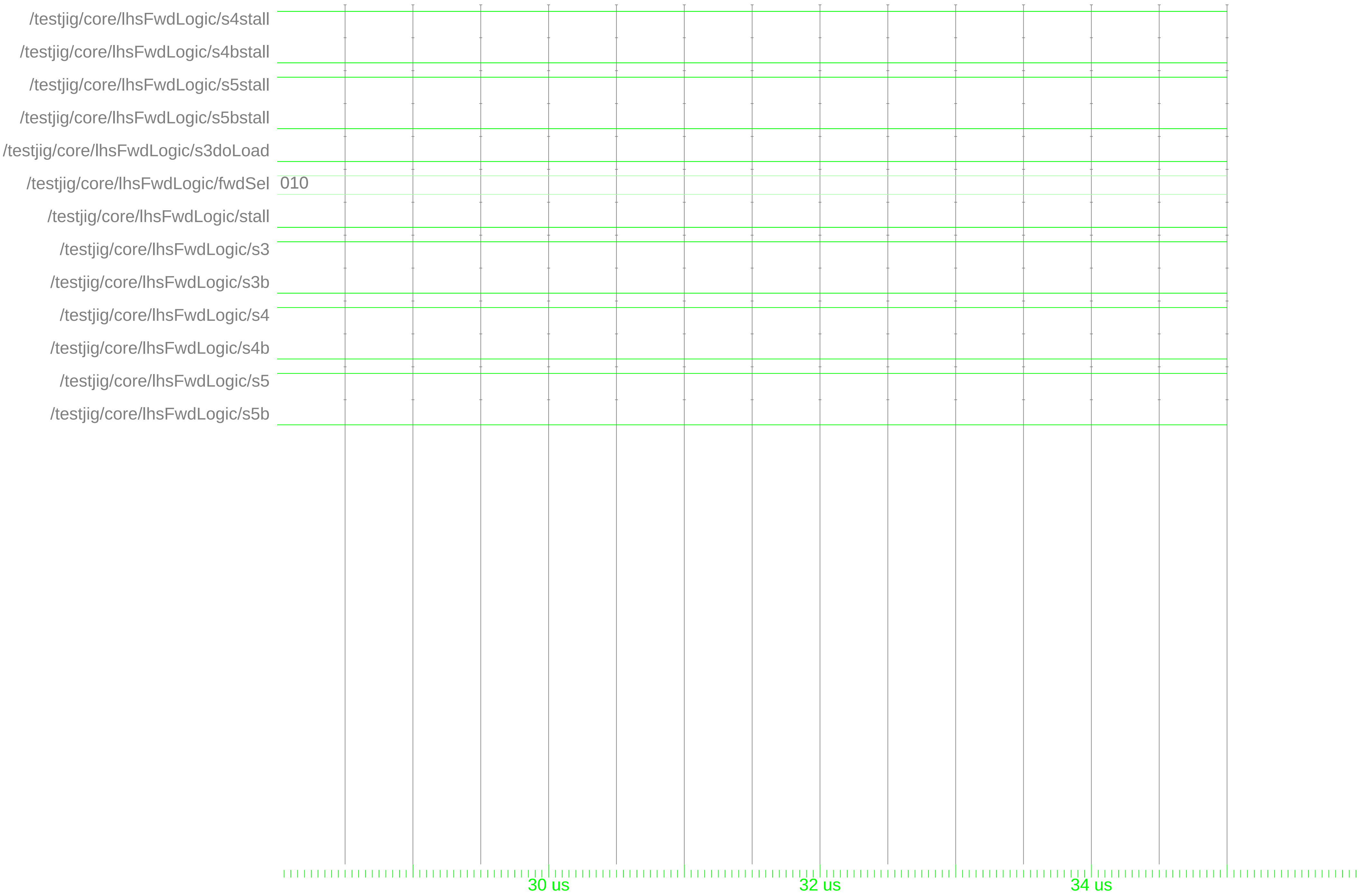

/testjig/core/lhsFwdLogic/s3brdNum 5
/testjig/core/lhsFwdLogic/s3rdNum 5
/testjig/core/lhsFwdLogic/s4brdNum 5
/testjig/core/lhsFwdLogic/s4rdNum 5
/testjig/core/lhsFwdLogic/s5brdNum 5
/testjig/core/lhsFwdLogic/s5rdNum 5
/testjig/core/s1stall
/testjig/core/s2stall
/testjig/core/s3stalled
/testjig/core/s4stalled
/testjig/core/s5stalled
/testjig/core/s1bstall
/testjig/core/s2bstall
/testjig/core/s3bstalled
/testjig/core/s4bstalled
/testjig/core/s5bstalled
-
/testjig/core/lhsFwdLogic/regNum 00101
/testjig/core/lhsFwdLogic/s3rdNum 00101
/testjig/core/lhsFwdLogic/s4rdNum 00101
/testjig/core/lhsFwdLogic/s5rdNum 00101
/testjig/core/lhsFwdLogic/s3brdNum 00101
/testjig/core/lhsFwdLogic/s4brdNum 00101
/testjig/core/lhsFwdLogic/s5brdNum 00101
/testjig/core/lhsFwdLogic/s3stall
/testjig/core/lhsFwdLogic/s3bstall
22 us
24 us
26 us
28 us

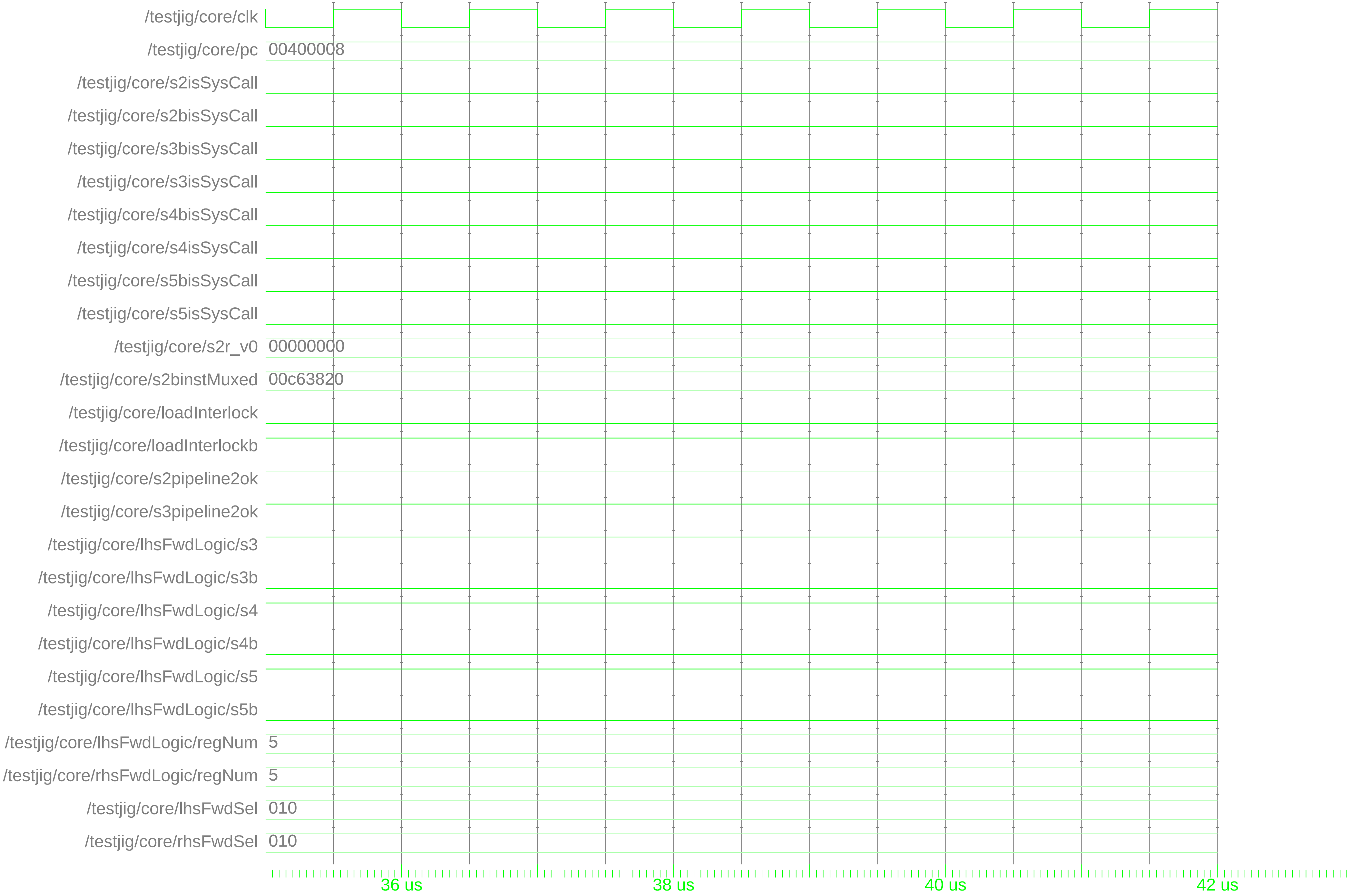

/testjig/core/lhsFwdLogic/s4stall
/testjig/core/lhsFwdLogic/s4bstall
/testjig/core/lhsFwdLogic/s5stall
/testjig/core/lhsFwdLogic/s5bstall
/testjig/core/lhsFwdLogic/s3doLoad
/testjig/core/lhsFwdLogic/fwdSel
010
/testjig/core/lhsFwdLogic/stall
/testjig/core/lhsFwdLogic/s3
/testjig/core/lhsFwdLogic/s3b
/testjig/core/lhsFwdLogic/s4
/testjig/core/lhsFwdLogic/s4b
/testjig/core/lhsFwdLogic/s5
/testjig/core/lhsFwdLogic/s5b
22 us
24 us
26 us
28 us

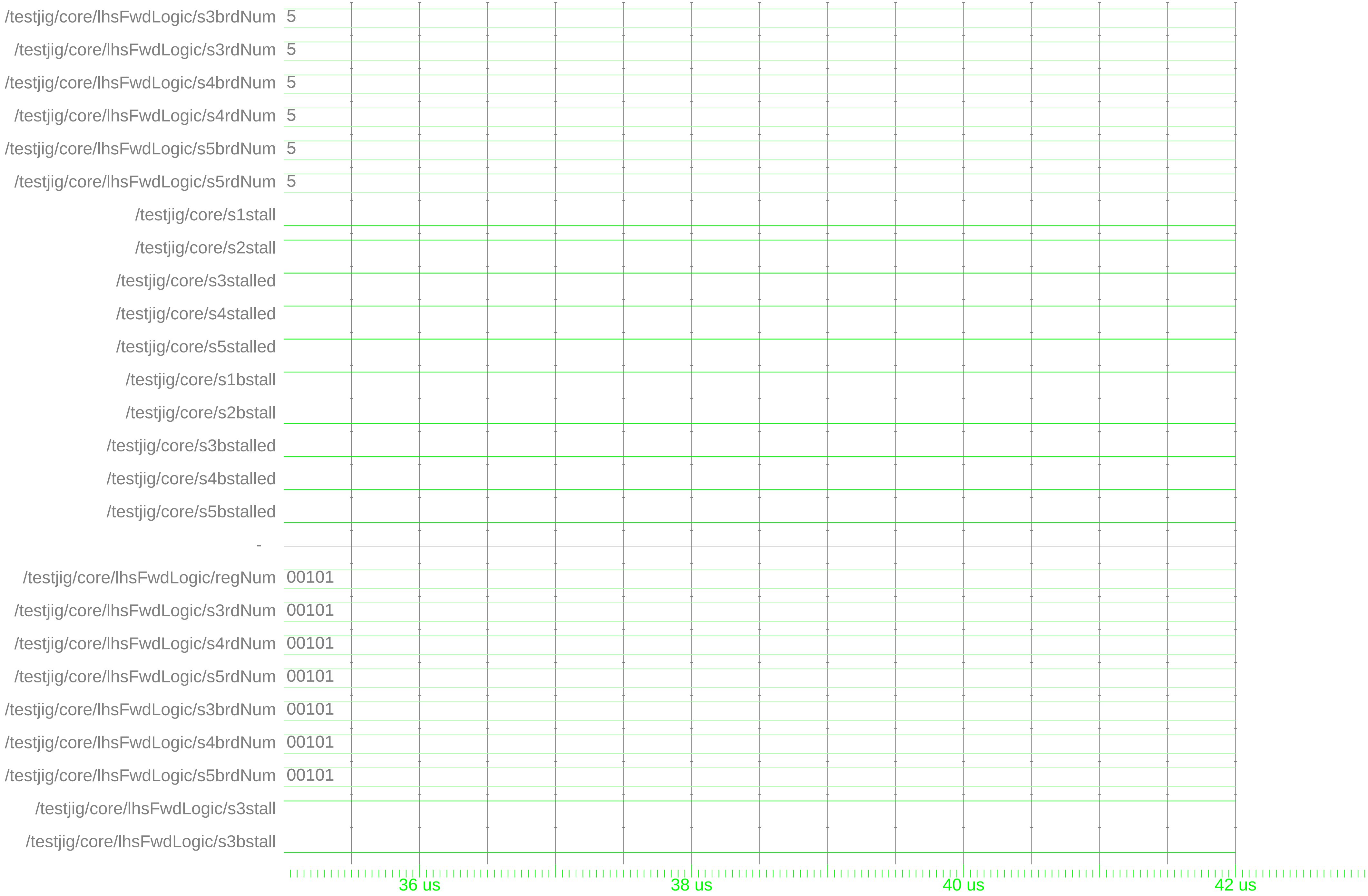


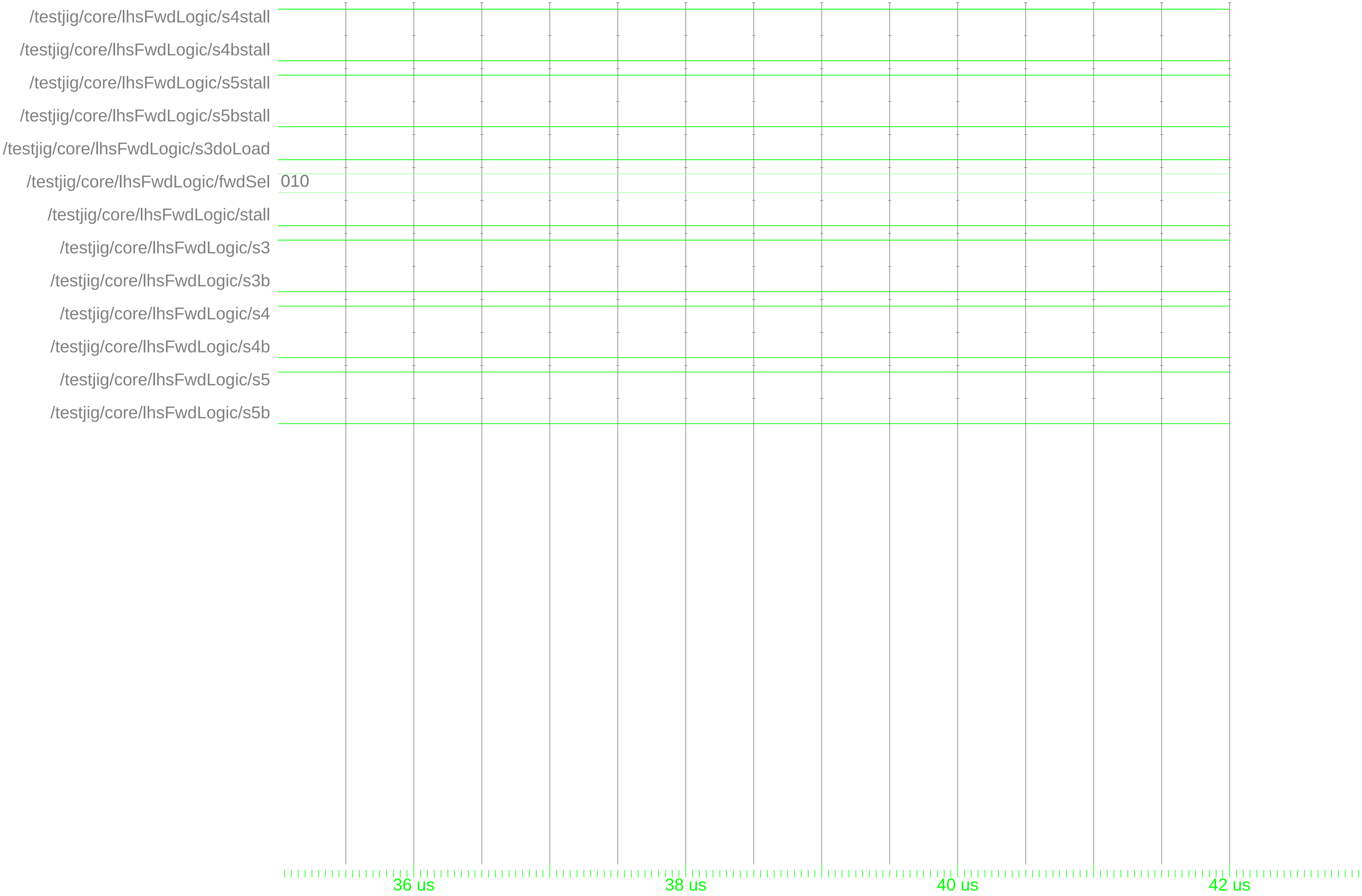
/testjig/core/clk
/testjig/core/pc
00400008
/testjig/core/s2isSysCall
/testjig/core/s2bisSysCall
/testjig/core/s3bisSysCall
/testjig/core/s3isSysCall
/testjig/core/s4bisSysCall
/testjig/core/s4isSysCall
/testjig/core/s5bisSysCall
/testjig/core/s5isSysCall
/testjig/core/s2r_v0
00000000
/testjig/core/s2binstMuxed
00c63820
/testjig/core/loadInterlock
/testjig/core/loadInterlockb
/testjig/core/s2pipeline2ok
/testjig/core/s3pipeline2ok
/testjig/core/lhsFwdLogic/s3
/testjig/core/lhsFwdLogic/s3b
/testjig/core/lhsFwdLogic/s4
/testjig/core/lhsFwdLogic/s4b
/testjig/core/lhsFwdLogic/s5
/testjig/core/lhsFwdLogic/s5b
/testjig/core/lhsFwdLogic/regNum
5
/testjig/core/rhsFwdLogic/regNum
5
/testjig/core/lhsFwdSel
010
/testjig/core/rhsFwdSel
010
30 us
32 us
34 us

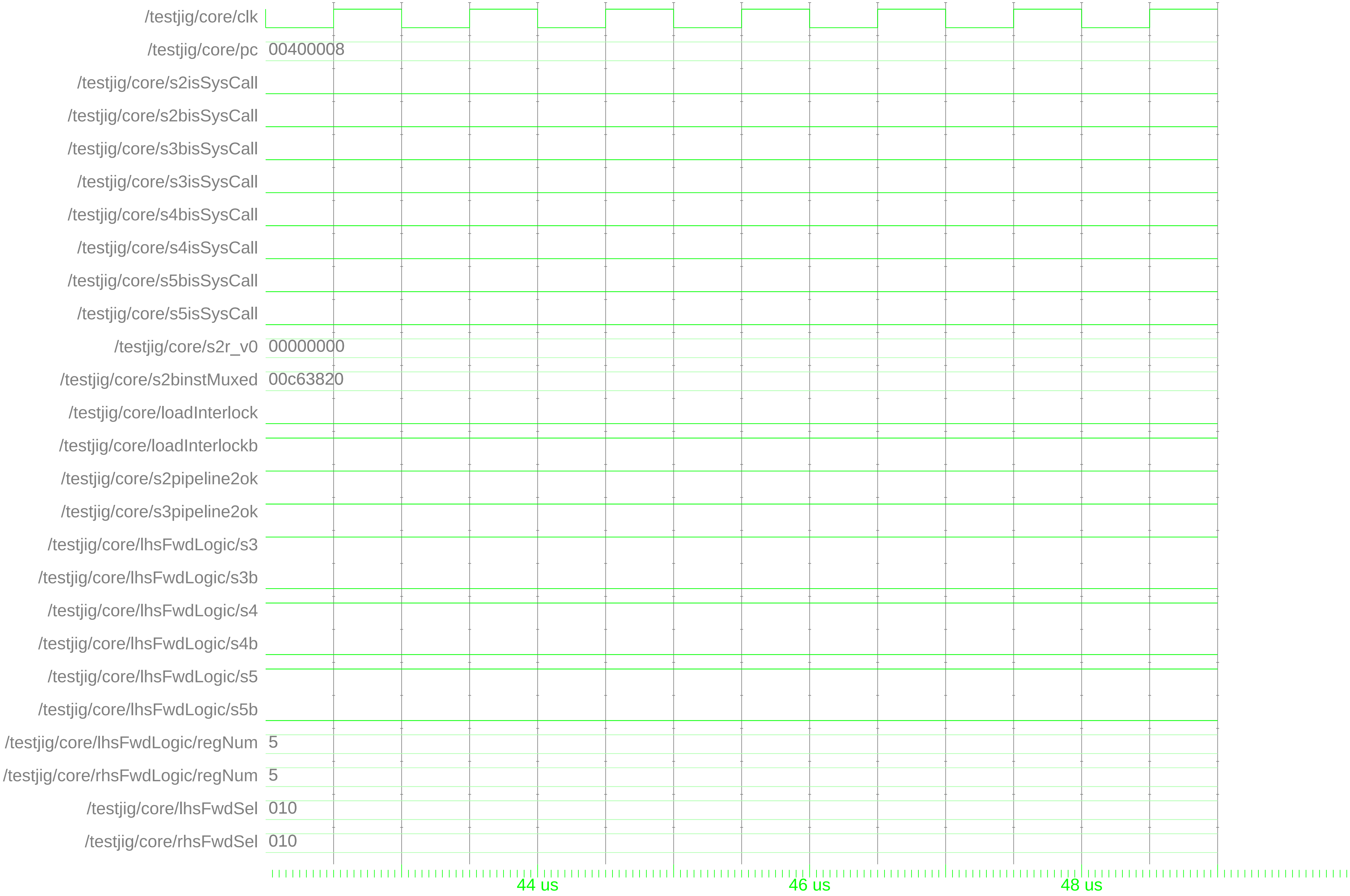

/testjig/core/lhsFwdLogic/s3brdNum 5
/testjig/core/lhsFwdLogic/s3rdNum 5
/testjig/core/lhsFwdLogic/s4brdNum 5
/testjig/core/lhsFwdLogic/s4rdNum 5
/testjig/core/lhsFwdLogic/s5brdNum 5
/testjig/core/lhsFwdLogic/s5rdNum 5
/testjig/core/s1stall
/testjig/core/s2stall
/testjig/core/s3stalled
/testjig/core/s4stalled
/testjig/core/s5stalled
/testjig/core/s1bstall
/testjig/core/s2bstall
/testjig/core/s3bstalled
/testjig/core/s4bstalled
/testjig/core/s5bstalled
-
/testjig/core/lhsFwdLogic/regNum 00101
/testjig/core/lhsFwdLogic/s3rdNum 00101
/testjig/core/lhsFwdLogic/s4rdNum 00101
/testjig/core/lhsFwdLogic/s5rdNum 00101
/testjig/core/lhsFwdLogic/s3brdNum 00101
/testjig/core/lhsFwdLogic/s4brdNum 00101
/testjig/core/lhsFwdLogic/s5brdNum 00101
/testjig/core/lhsFwdLogic/s3stall
/testjig/core/lhsFwdLogic/s3bstall
30 us
32 us
34 us

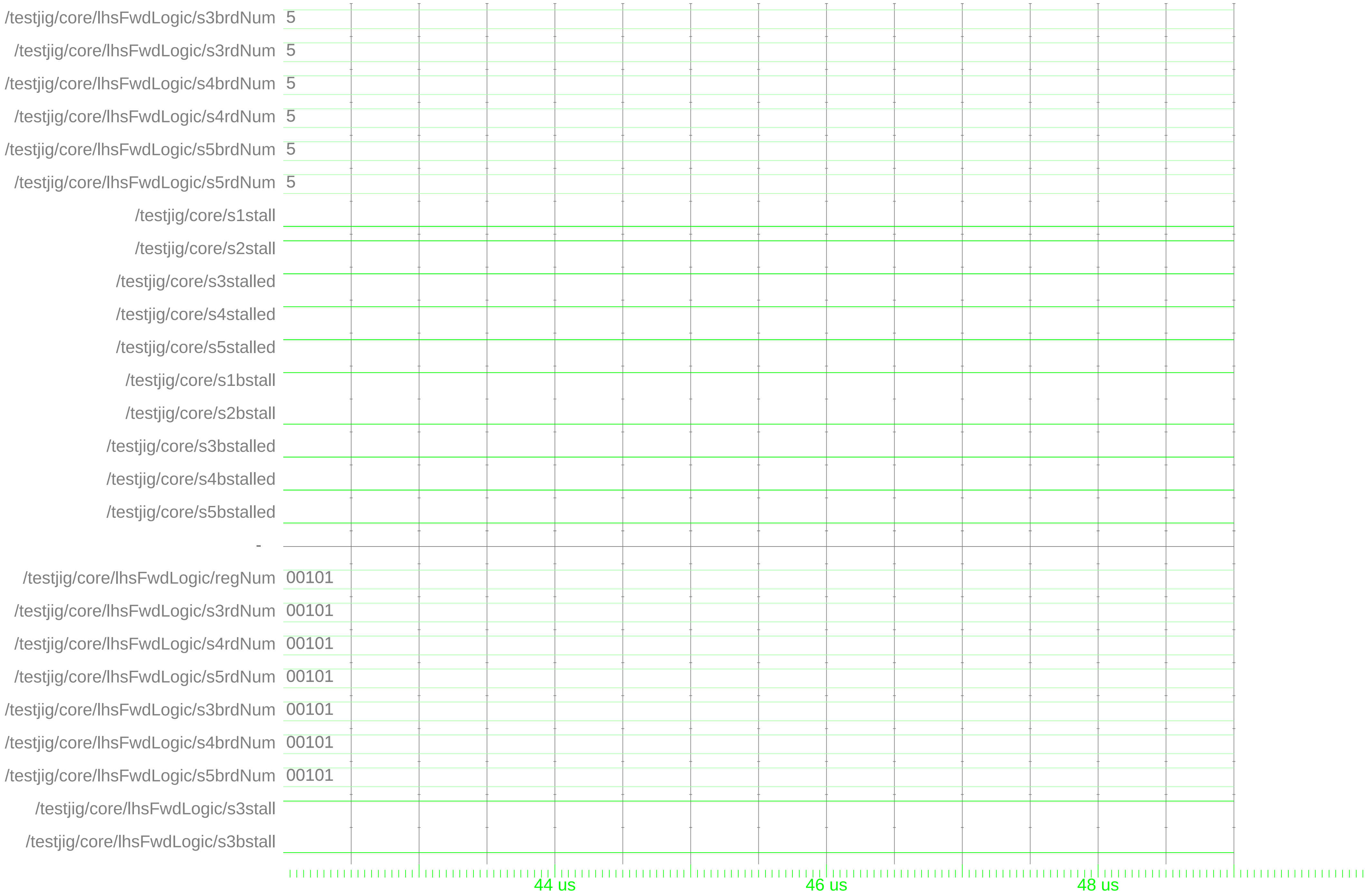

/testjig/core/lhsFwdLogic/s4stall
/testjig/core/lhsFwdLogic/s4bstall
/testjig/core/lhsFwdLogic/s5stall
/testjig/core/lhsFwdLogic/s5bstall
/testjig/core/lhsFwdLogic/s3doLoad
/testjig/core/lhsFwdLogic/fwdSel
010
/testjig/core/lhsFwdLogic/stall
/testjig/core/lhsFwdLogic/s3
/testjig/core/lhsFwdLogic/s3b
/testjig/core/lhsFwdLogic/s4
/testjig/core/lhsFwdLogic/s4b
/testjig/core/lhsFwdLogic/s5
/testjig/core/lhsFwdLogic/s5b
30 us
32 us
34 us

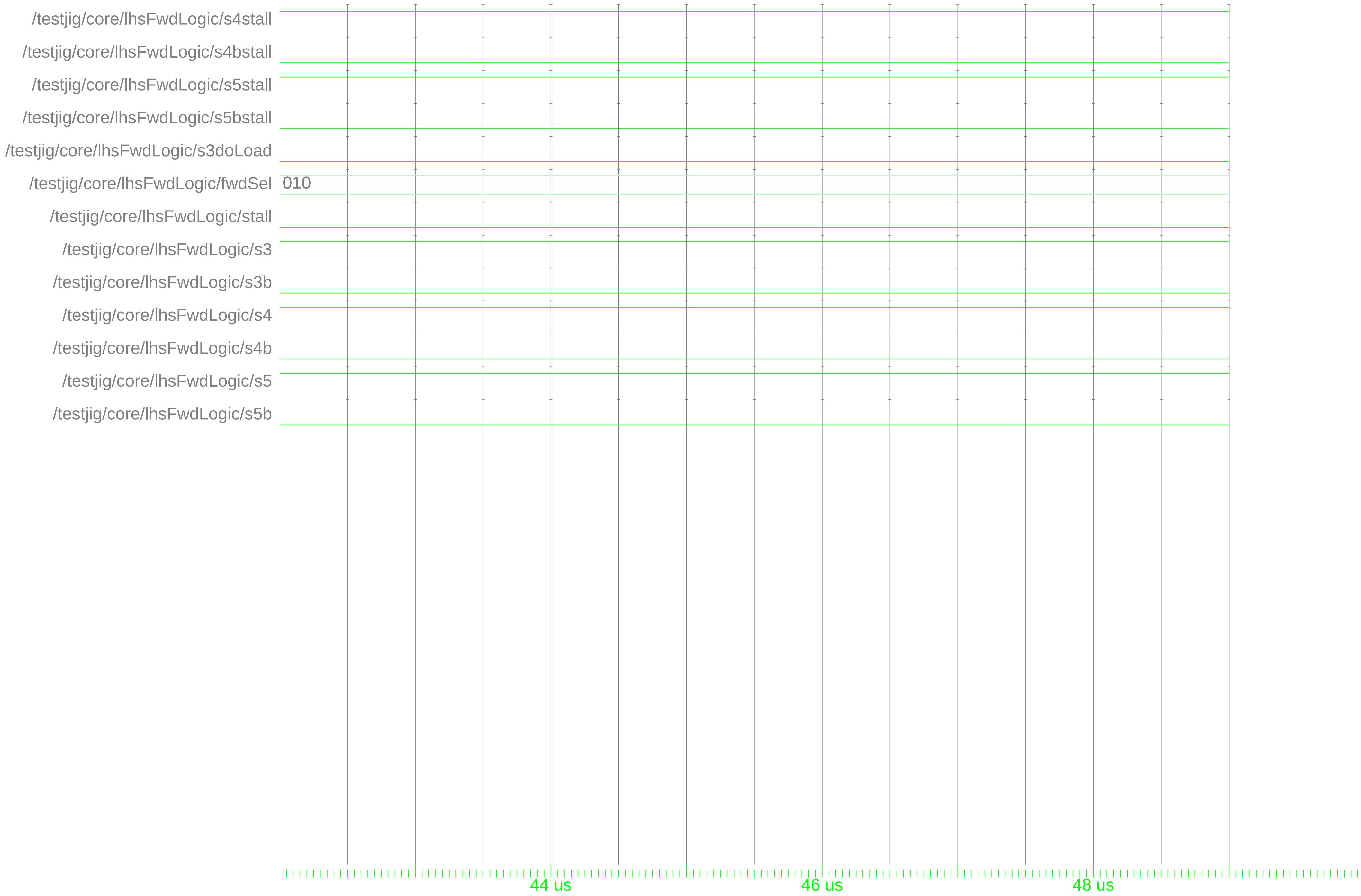

/testjig/core/clk
/testjig/core/pc
00400008
/testjig/core/s2isSysCall
/testjig/core/s2bisSysCall
/testjig/core/s3bisSysCall
/testjig/core/s3isSysCall
/testjig/core/s4bisSysCall
/testjig/core/s4isSysCall
/testjig/core/s5bisSysCall
/testjig/core/s5isSysCall
/testjig/core/s2r_v0
00000000
/testjig/core/s2binstMuxed
00c63820
/testjig/core/loadInterlock
/testjig/core/loadInterlockb
/testjig/core/s2pipeline2ok
/testjig/core/s3pipeline2ok
/testjig/core/lhsFwdLogic/s3
/testjig/core/lhsFwdLogic/s3b
/testjig/core/lhsFwdLogic/s4
/testjig/core/lhsFwdLogic/s4b
/testjig/core/lhsFwdLogic/s5
/testjig/core/lhsFwdLogic/s5b
/testjig/core/lhsFwdLogic/regNum
5
/testjig/core/rhsFwdLogic/regNum
5
/testjig/core/lhsFwdSel
010
/testjig/core/rhsFwdSel
010
36 us
38 us
40 us
42 us

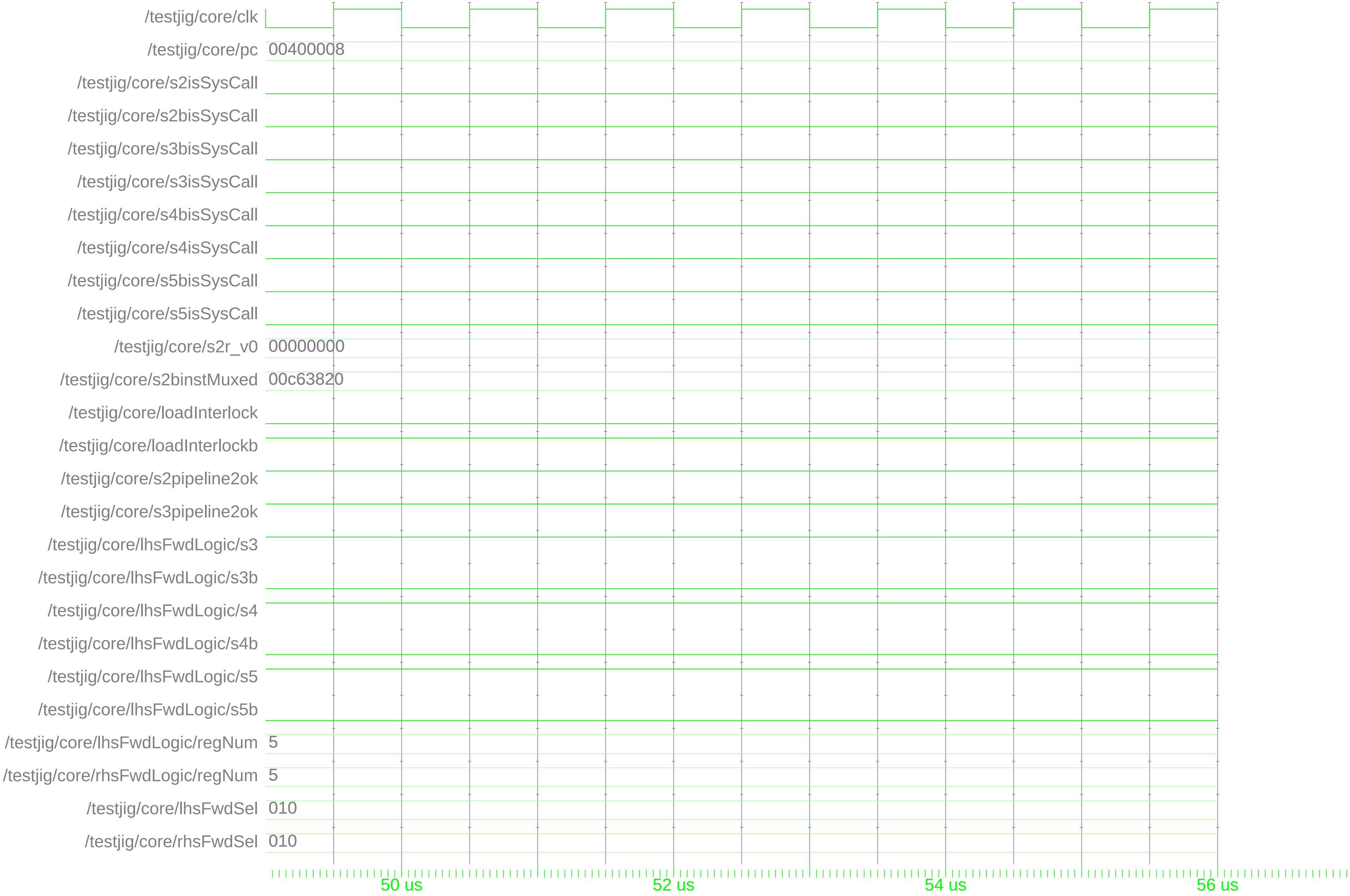

/testjig/core/lhsFwdLogic/s3brdNum 5
/testjig/core/lhsFwdLogic/s3rdNum 5
/testjig/core/lhsFwdLogic/s4brdNum 5
/testjig/core/lhsFwdLogic/s4rdNum 5
/testjig/core/lhsFwdLogic/s5brdNum 5
/testjig/core/lhsFwdLogic/s5rdNum 5
/testjig/core/s1stall
/testjig/core/s2stall
/testjig/core/s3stalled
/testjig/core/s4stalled
/testjig/core/s5stalled
/testjig/core/s1bstall
/testjig/core/s2bstall
/testjig/core/s3bstalled
/testjig/core/s4bstalled
/testjig/core/s5bstalled
-
/testjig/core/lhsFwdLogic/regNum 00101
/testjig/core/lhsFwdLogic/s3rdNum 00101
/testjig/core/lhsFwdLogic/s4rdNum 00101
/testjig/core/lhsFwdLogic/s5rdNum 00101
/testjig/core/lhsFwdLogic/s3brdNum 00101
/testjig/core/lhsFwdLogic/s4brdNum 00101
/testjig/core/lhsFwdLogic/s5brdNum 00101
/testjig/core/lhsFwdLogic/s3stall
/testjig/core/lhsFwdLogic/s3bstall
36 us
38 us
40 us
42 us

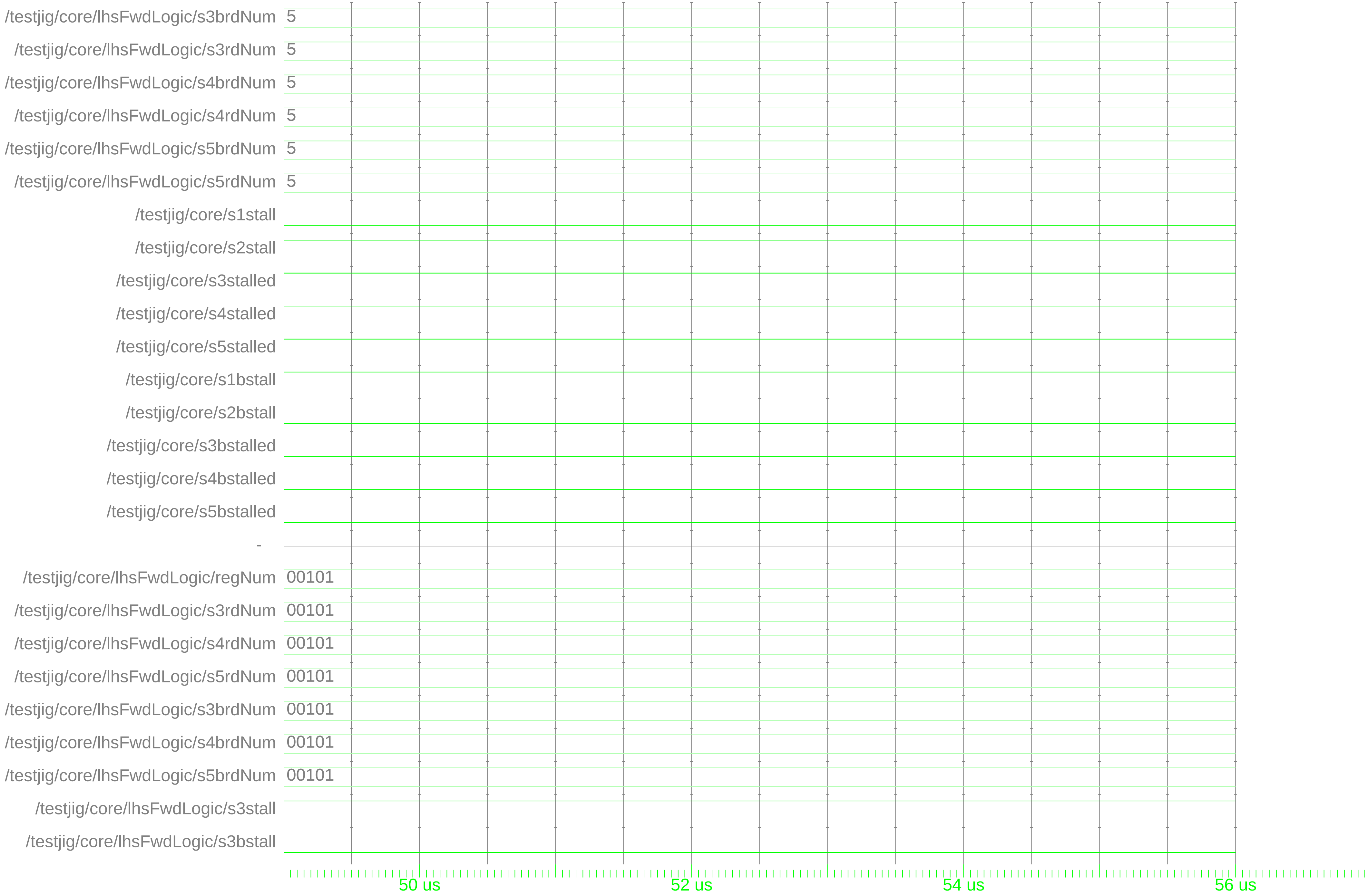

/testjig/core/lhsFwdLogic/s4stall
/testjig/core/lhsFwdLogic/s4bstall
/testjig/core/lhsFwdLogic/s5stall
/testjig/core/lhsFwdLogic/s5bstall
/testjig/core/lhsFwdLogic/s3doLoad
/testjig/core/lhsFwdLogic/fwdSel
010
/testjig/core/lhsFwdLogic/stall
/testjig/core/lhsFwdLogic/s3
/testjig/core/lhsFwdLogic/s3b
/testjig/core/lhsFwdLogic/s4
/testjig/core/lhsFwdLogic/s4b
/testjig/core/lhsFwdLogic/s5
/testjig/core/lhsFwdLogic/s5b
36 us
38 us
40 us
42 us

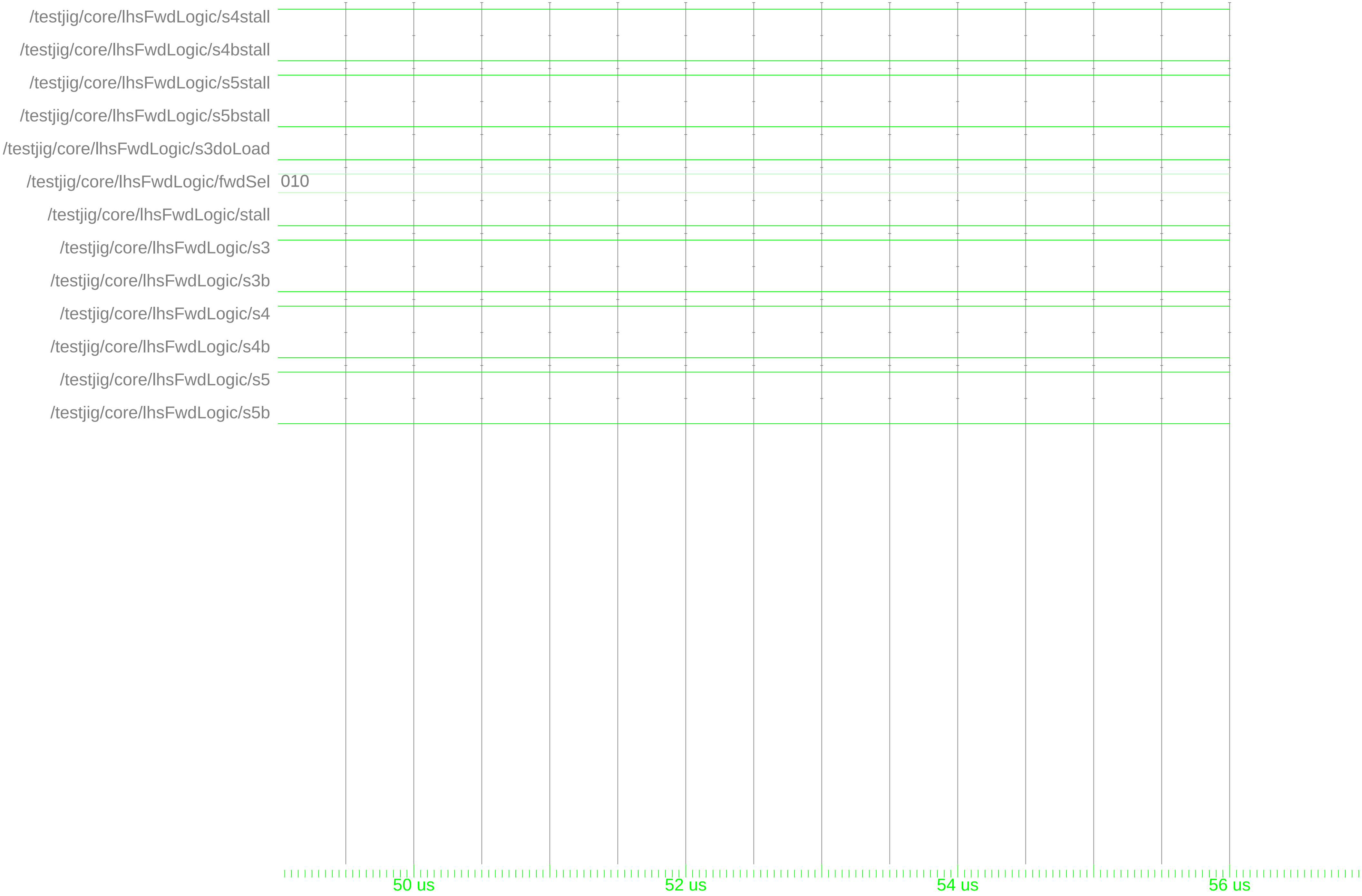

/testjig/core/clk
/testjig/core/pc
00400008
/testjig/core/s2isSysCall
/testjig/core/s2bisSysCall
/testjig/core/s3bisSysCall
/testjig/core/s3isSysCall
/testjig/core/s4bisSysCall
/testjig/core/s4isSysCall
/testjig/core/s5bisSysCall
/testjig/core/s5isSysCall
/testjig/core/s2r_v0
00000000
/testjig/core/s2binstMuxed
00c63820
/testjig/core/loadInterlock
/testjig/core/loadInterlockb
/testjig/core/s2pipeline2ok
/testjig/core/s3pipeline2ok
/testjig/core/lhsFwdLogic/s3
/testjig/core/lhsFwdLogic/s3b
/testjig/core/lhsFwdLogic/s4
/testjig/core/lhsFwdLogic/s4b
/testjig/core/lhsFwdLogic/s5
/testjig/core/lhsFwdLogic/s5b
/testjig/core/lhsFwdLogic/regNum
5
/testjig/core/rhsFwdLogic/regNum
5
/testjig/core/lhsFwdSel
010
/testjig/core/rhsFwdSel
010
44 us
46 us
48 us

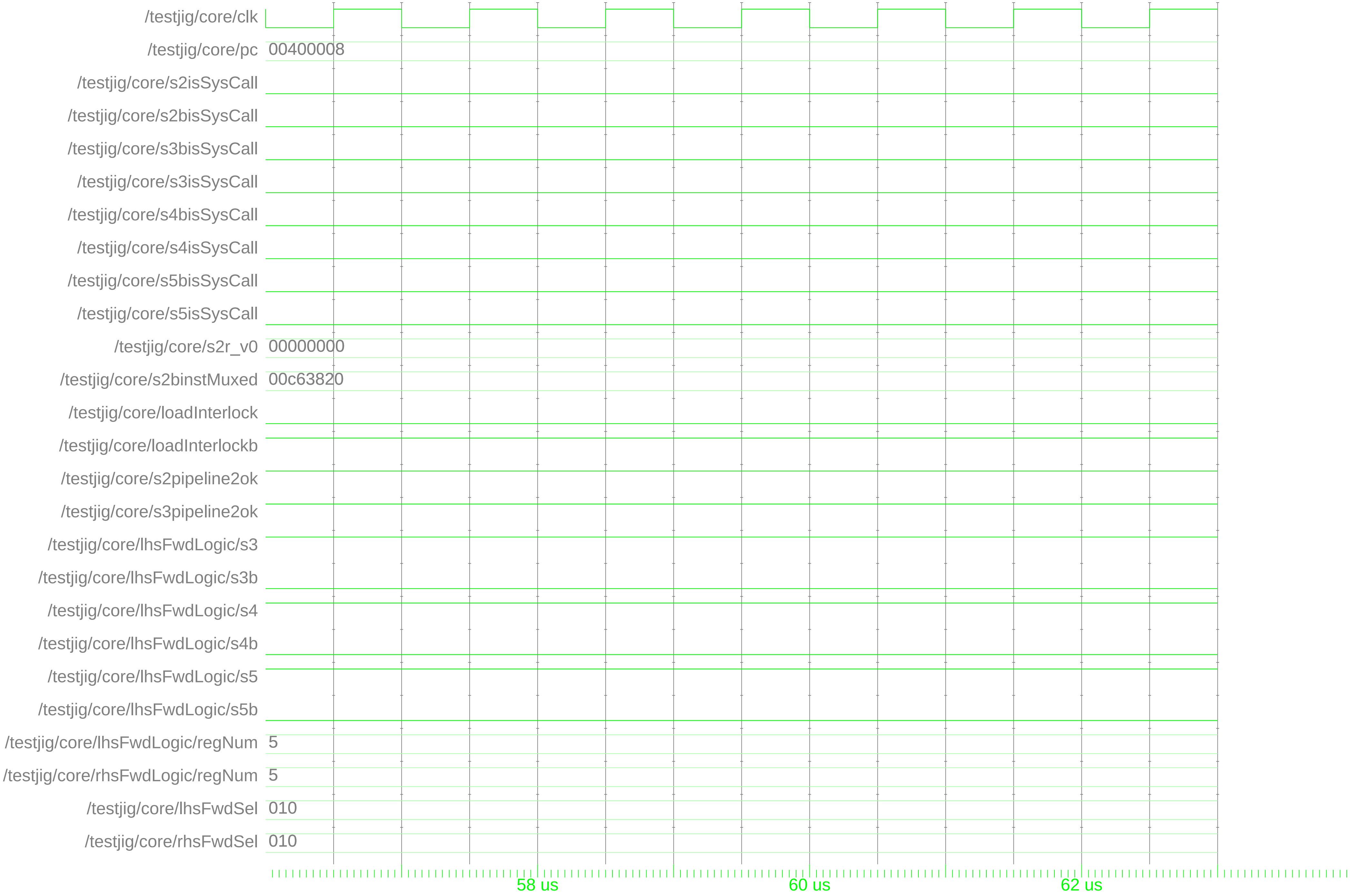

/testjig/core/lhsFwdLogic/s3brdNum 5
/testjig/core/lhsFwdLogic/s3rdNum 5
/testjig/core/lhsFwdLogic/s4brdNum 5
/testjig/core/lhsFwdLogic/s4rdNum 5
/testjig/core/lhsFwdLogic/s5brdNum 5
/testjig/core/lhsFwdLogic/s5rdNum 5
/testjig/core/s1stall
/testjig/core/s2stall
/testjig/core/s3stalled
/testjig/core/s4stalled
/testjig/core/s5stalled
/testjig/core/s1bstall
/testjig/core/s2bstall
/testjig/core/s3bstalled
/testjig/core/s4bstalled
/testjig/core/s5bstalled
-
/testjig/core/lhsFwdLogic/regNum 00101
/testjig/core/lhsFwdLogic/s3rdNum 00101
/testjig/core/lhsFwdLogic/s4rdNum 00101
/testjig/core/lhsFwdLogic/s5rdNum 00101
/testjig/core/lhsFwdLogic/s3brdNum 00101
/testjig/core/lhsFwdLogic/s4brdNum 00101
/testjig/core/lhsFwdLogic/s5brdNum 00101
/testjig/core/lhsFwdLogic/s3stall
/testjig/core/lhsFwdLogic/s3bstall
44 us
46 us
48 us

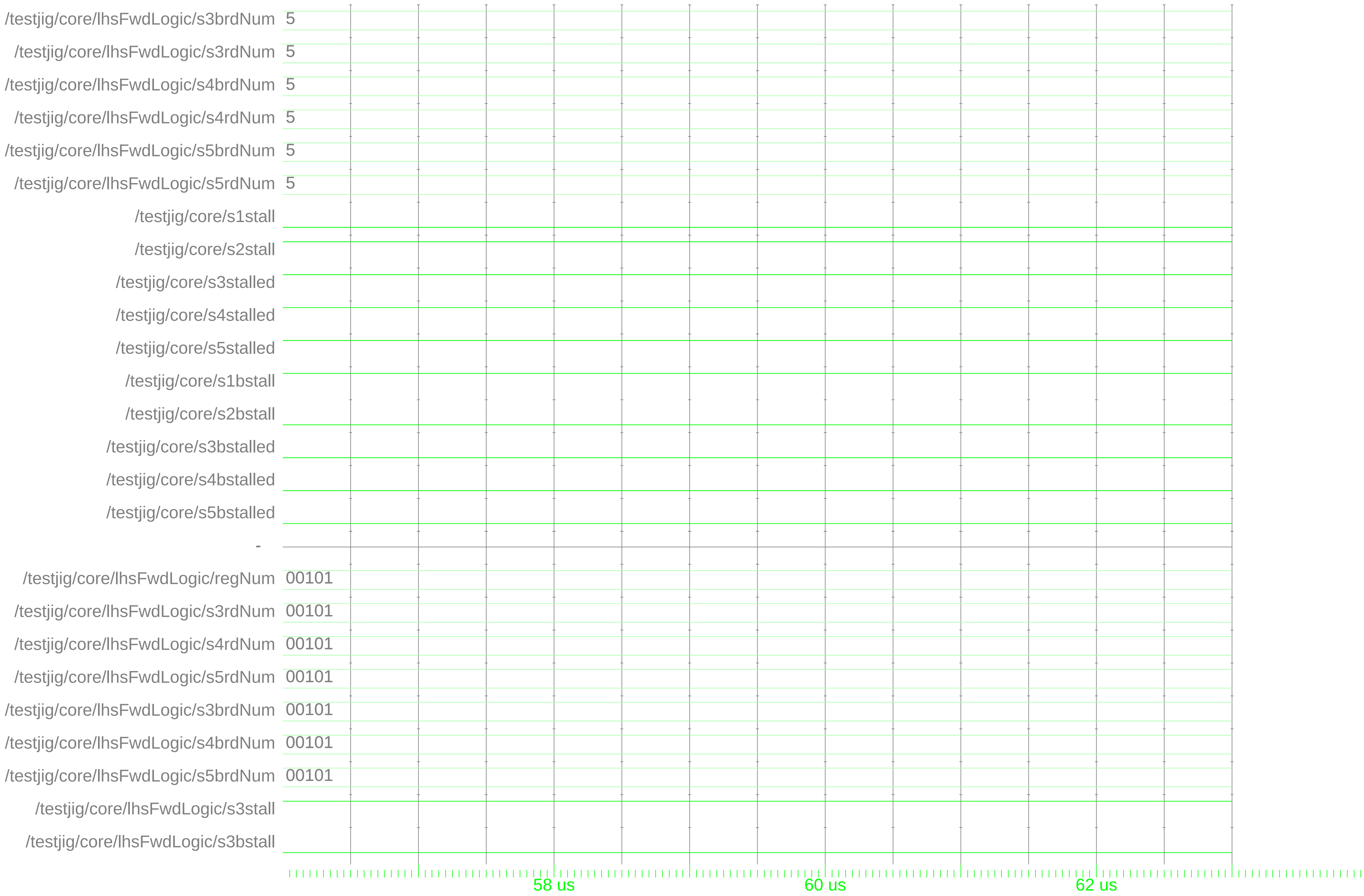

/testjig/core/lhsFwdLogic/s4stall
/testjig/core/lhsFwdLogic/s4bstall
/testjig/core/lhsFwdLogic/s5stall
/testjig/core/lhsFwdLogic/s5bstall
/testjig/core/lhsFwdLogic/s3doLoad
/testjig/core/lhsFwdLogic/fwdSel
010
/testjig/core/lhsFwdLogic/stall
/testjig/core/lhsFwdLogic/s3
/testjig/core/lhsFwdLogic/s3b
/testjig/core/lhsFwdLogic/s4
/testjig/core/lhsFwdLogic/s4b
/testjig/core/lhsFwdLogic/s5
/testjig/core/lhsFwdLogic/s5b
44 us
46 us
48 us

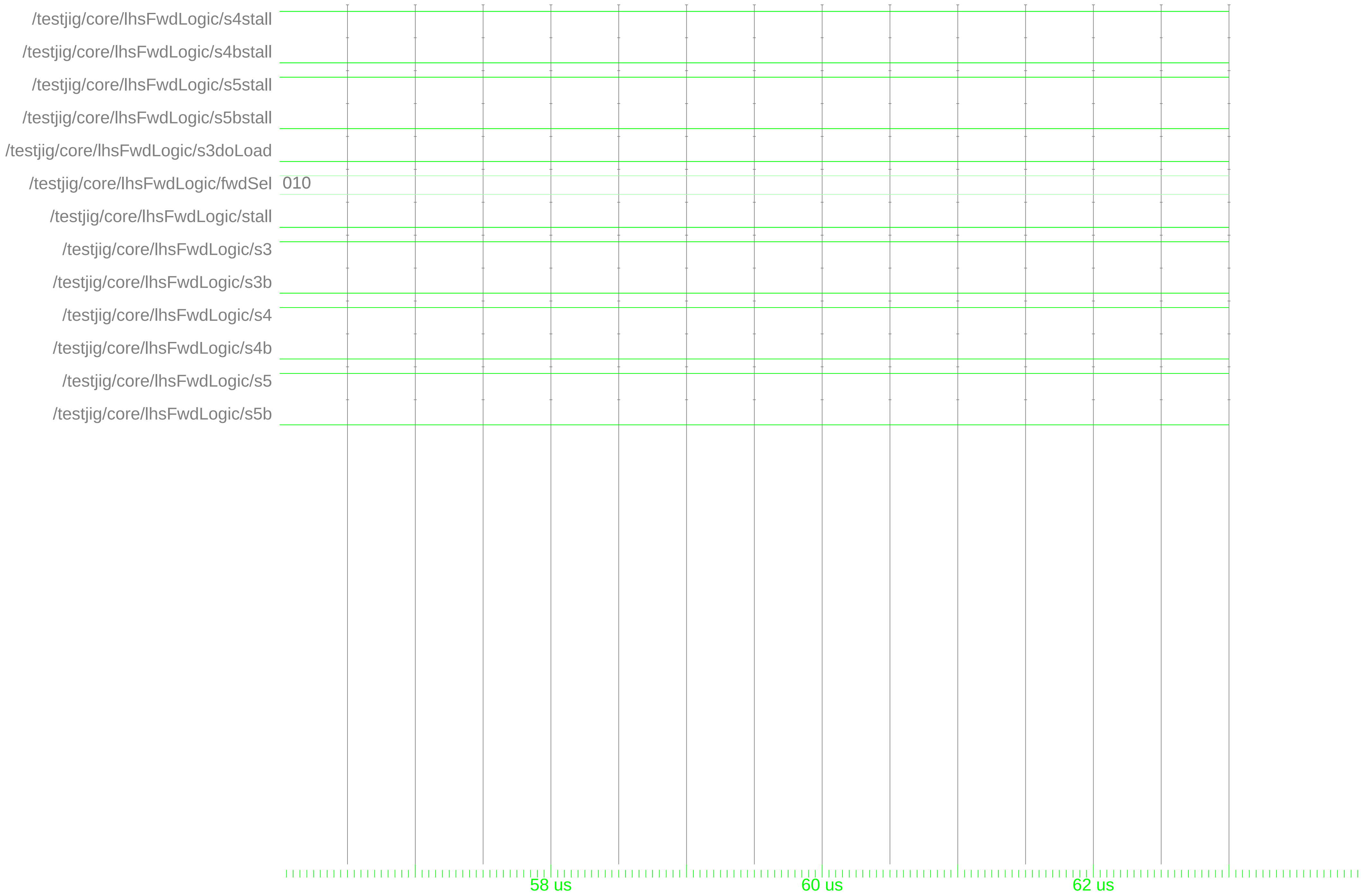

/testjig/core/clk
/testjig/core/pc
00400008
/testjig/core/s2isSysCall
/testjig/core/s2bisSysCall
/testjig/core/s3bisSysCall
/testjig/core/s3isSysCall
/testjig/core/s4bisSysCall
/testjig/core/s4isSysCall
/testjig/core/s5bisSysCall
/testjig/core/s5isSysCall
/testjig/core/s2r_v0
00000000
/testjig/core/s2binstMuxed
00c63820
/testjig/core/loadInterlock
/testjig/core/loadInterlockb
/testjig/core/s2pipeline2ok
/testjig/core/s3pipeline2ok
/testjig/core/lhsFwdLogic/s3
/testjig/core/lhsFwdLogic/s3b
/testjig/core/lhsFwdLogic/s4
/testjig/core/lhsFwdLogic/s4b
/testjig/core/lhsFwdLogic/s5
/testjig/core/lhsFwdLogic/s5b
/testjig/core/lhsFwdLogic/regNum
5
/testjig/core/rhsFwdLogic/regNum
5
/testjig/core/lhsFwdSel
010
/testjig/core/rhsFwdSel
010
50 us
52 us
54 us
56 us

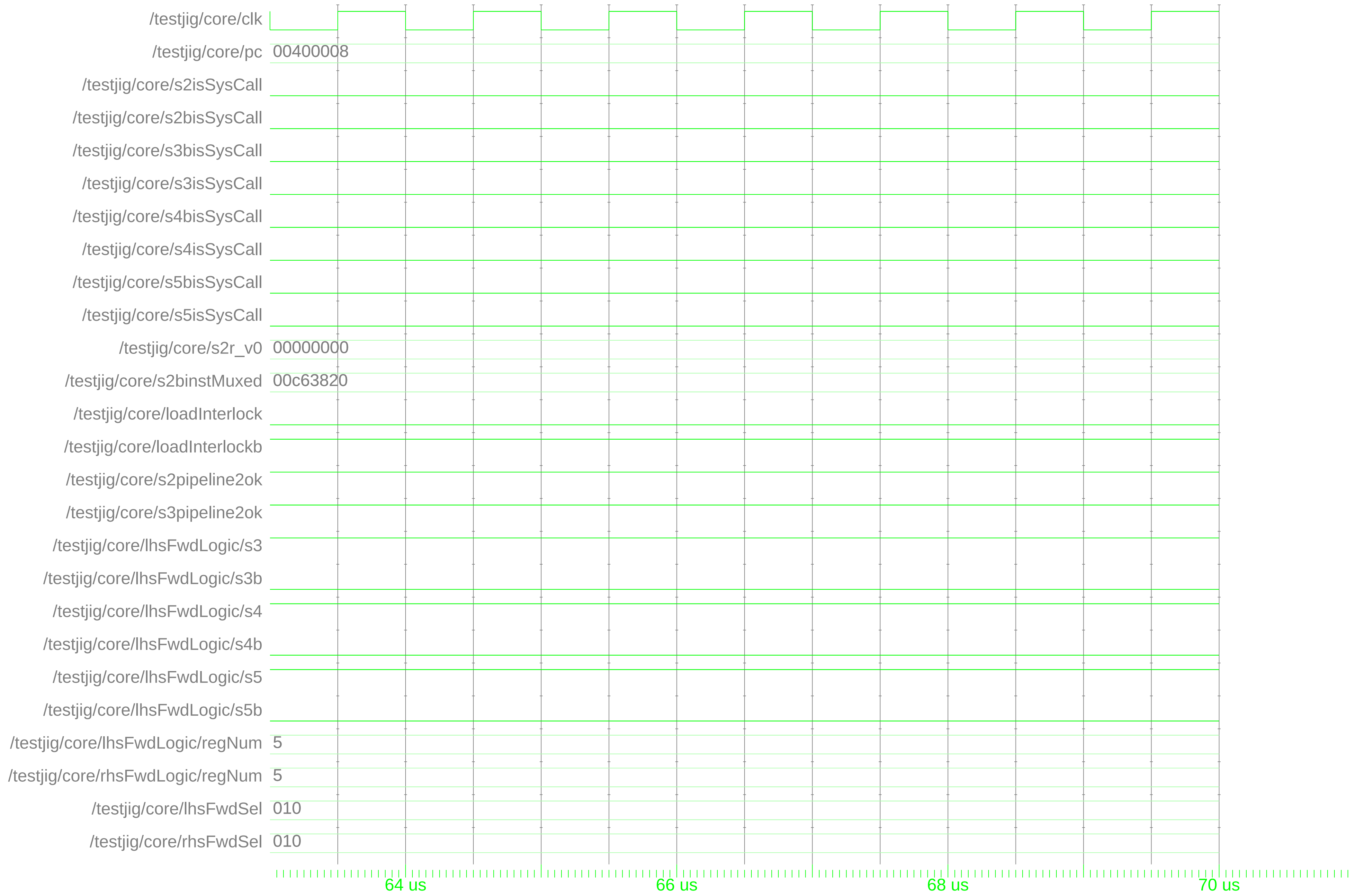

/testjig/core/lhsFwdLogic/s3brdNum 5
/testjig/core/lhsFwdLogic/s3rdNum 5
/testjig/core/lhsFwdLogic/s4brdNum 5
/testjig/core/lhsFwdLogic/s4rdNum 5
/testjig/core/lhsFwdLogic/s5brdNum 5
/testjig/core/lhsFwdLogic/s5rdNum 5
/testjig/core/s1stall
/testjig/core/s2stall
/testjig/core/s3stalled
/testjig/core/s4stalled
/testjig/core/s5stalled
/testjig/core/s1bstall
/testjig/core/s2bstall
/testjig/core/s3bstalled
/testjig/core/s4bstalled
/testjig/core/s5bstalled
-
/testjig/core/lhsFwdLogic/regNum 00101
/testjig/core/lhsFwdLogic/s3rdNum 00101
/testjig/core/lhsFwdLogic/s4rdNum 00101
/testjig/core/lhsFwdLogic/s5rdNum 00101
/testjig/core/lhsFwdLogic/s3brdNum 00101
/testjig/core/lhsFwdLogic/s4brdNum 00101
/testjig/core/lhsFwdLogic/s5brdNum 00101
/testjig/core/lhsFwdLogic/s3stall
/testjig/core/lhsFwdLogic/s3bstall
50 us
52 us
54 us
56 us

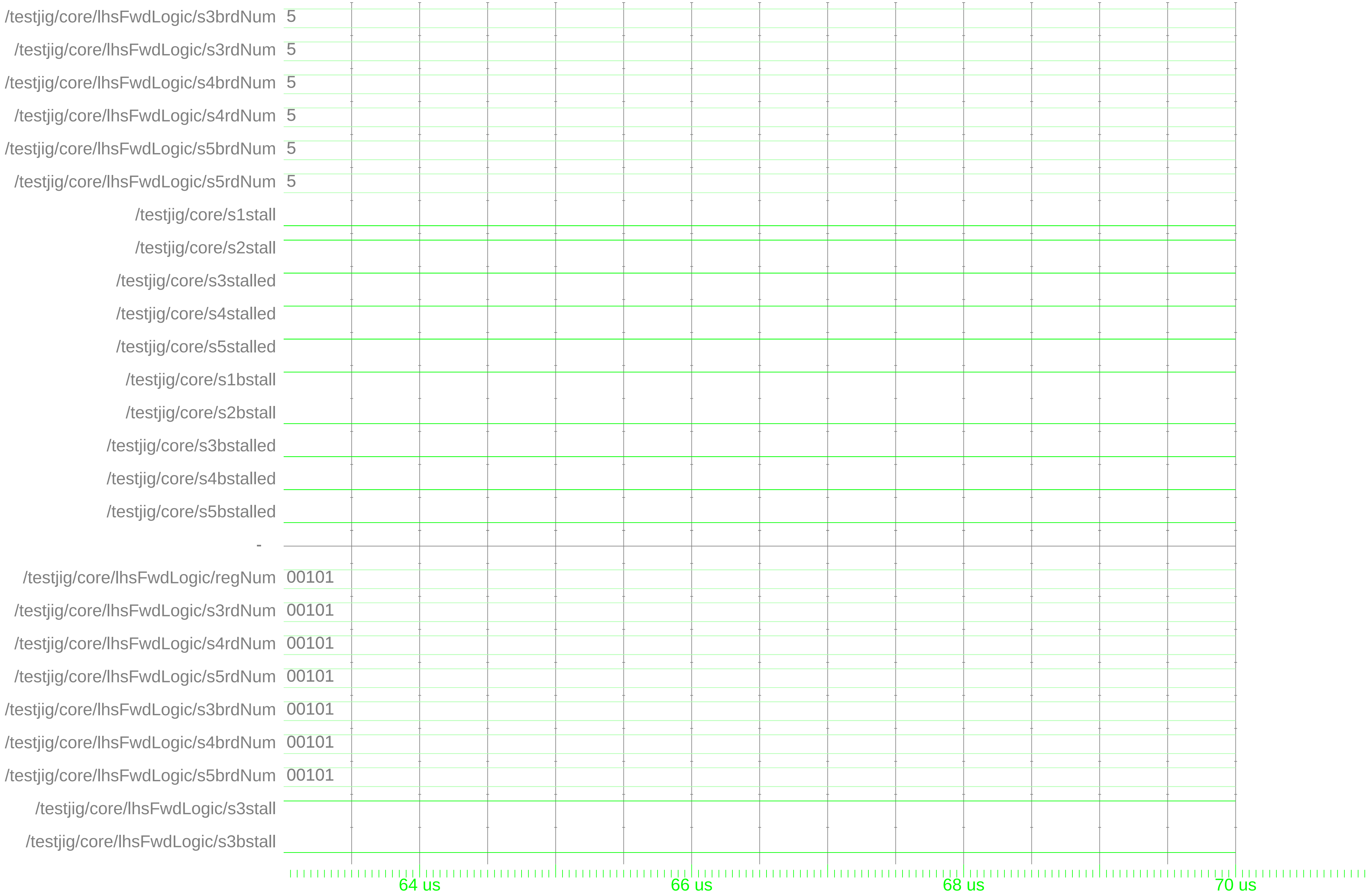

/testjig/core/lhsFwdLogic/s4stall
/testjig/core/lhsFwdLogic/s4bstall
/testjig/core/lhsFwdLogic/s5stall
/testjig/core/lhsFwdLogic/s5bstall
/testjig/core/lhsFwdLogic/s3doLoad
/testjig/core/lhsFwdLogic/fwdSel
010
/testjig/core/lhsFwdLogic/stall
/testjig/core/lhsFwdLogic/s3
/testjig/core/lhsFwdLogic/s3b
/testjig/core/lhsFwdLogic/s4
/testjig/core/lhsFwdLogic/s4b
/testjig/core/lhsFwdLogic/s5
/testjig/core/lhsFwdLogic/s5b
50 us
52 us
54 us
56 us

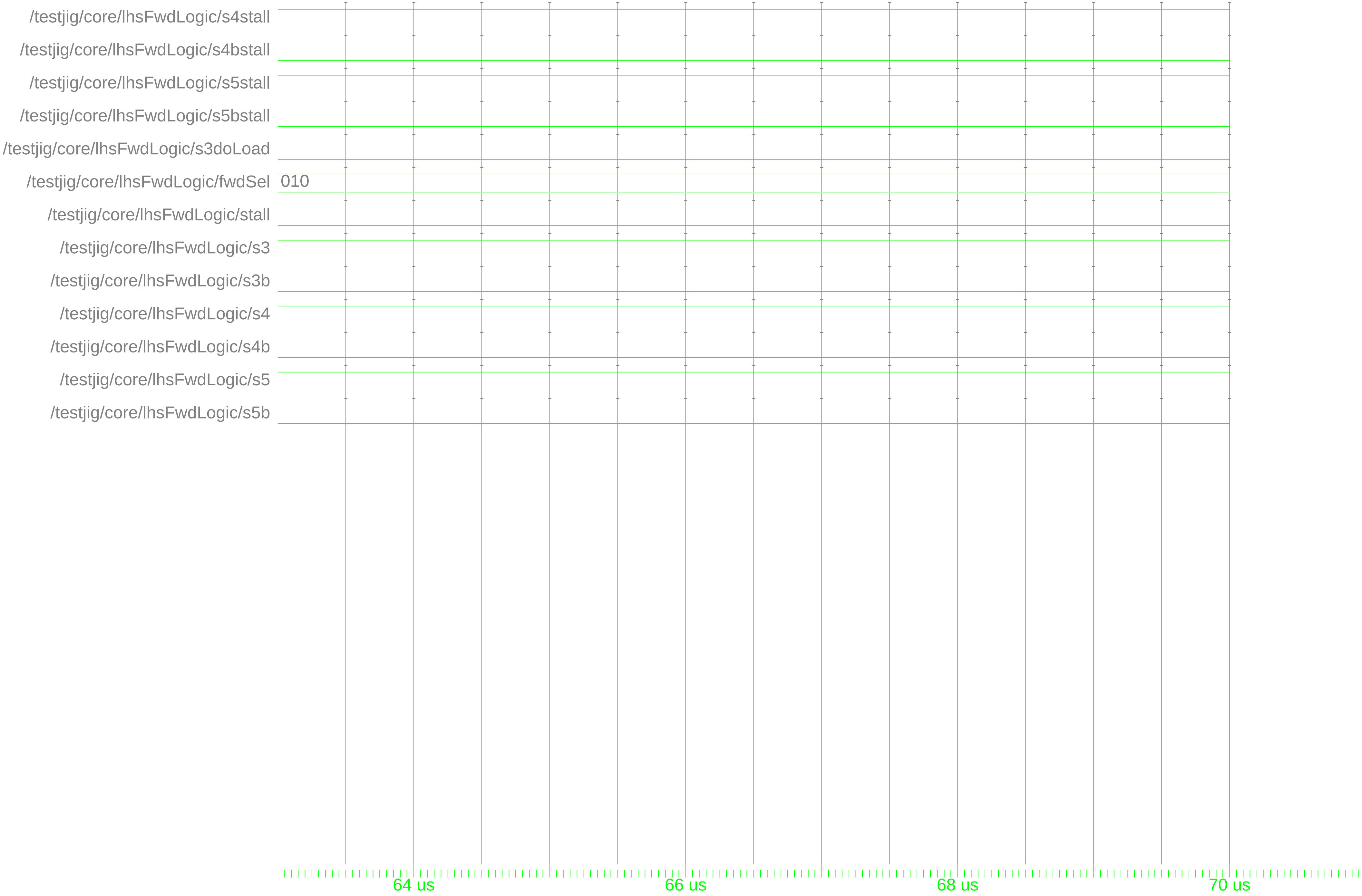

/testjig/core/clk
/testjig/core/pc
00400008
/testjig/core/s2isSysCall
/testjig/core/s2bisSysCall
/testjig/core/s3bisSysCall
/testjig/core/s3isSysCall
/testjig/core/s4bisSysCall
/testjig/core/s4isSysCall
/testjig/core/s5bisSysCall
/testjig/core/s5isSysCall
/testjig/core/s2r_v0
00000000
/testjig/core/s2binstMuxed
00c63820
/testjig/core/loadInterlock
/testjig/core/loadInterlockb
/testjig/core/s2pipeline2ok
/testjig/core/s3pipeline2ok
/testjig/core/lhsFwdLogic/s3
/testjig/core/lhsFwdLogic/s3b
/testjig/core/lhsFwdLogic/s4
/testjig/core/lhsFwdLogic/s4b
/testjig/core/lhsFwdLogic/s5
/testjig/core/lhsFwdLogic/s5b
/testjig/core/lhsFwdLogic/regNum
5
/testjig/core/rhsFwdLogic/regNum
5
/testjig/core/lhsFwdSel
010
/testjig/core/rhsFwdSel
010
58 us
60 us
62 us

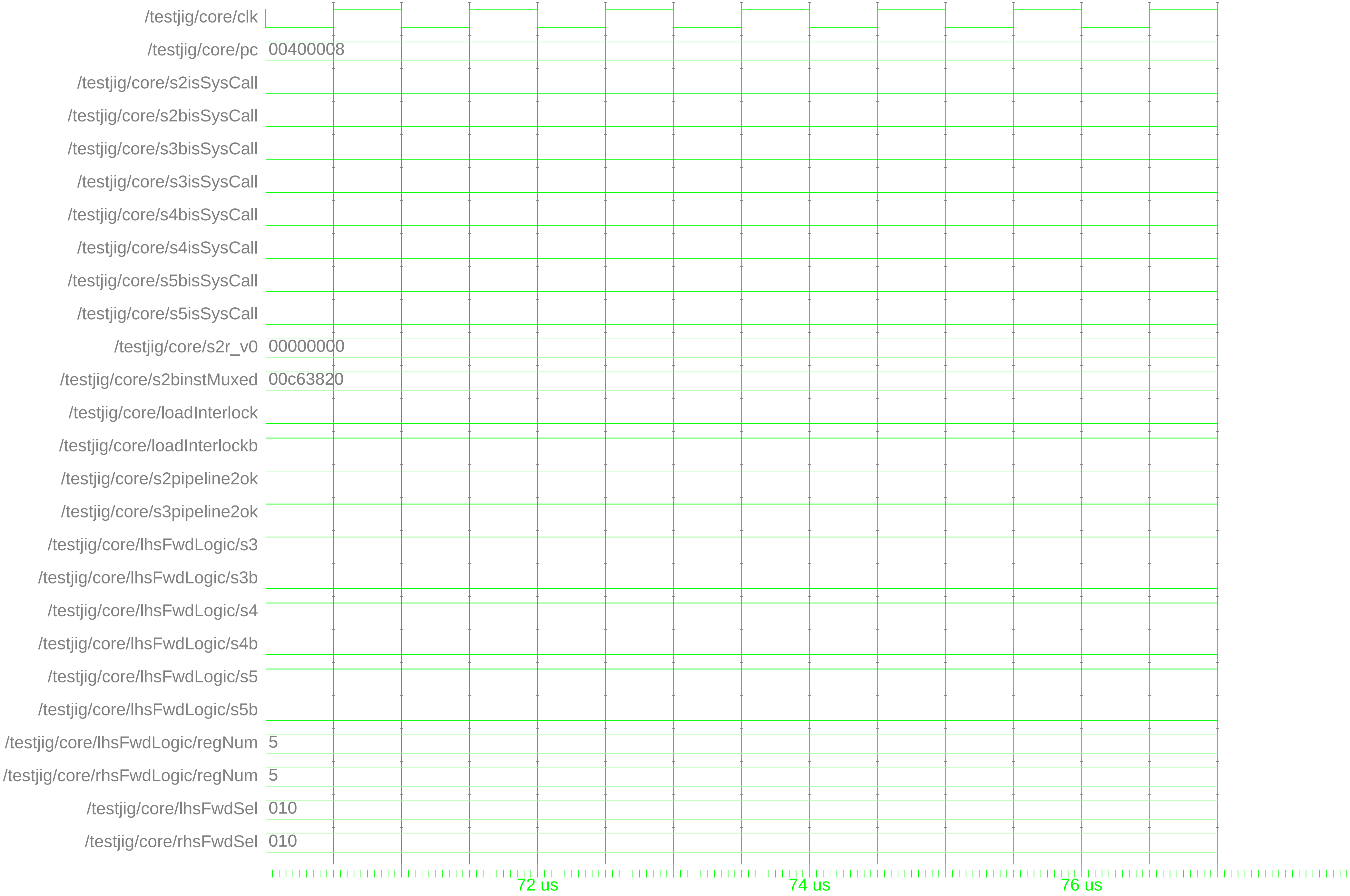

/testjig/core/lhsFwdLogic/s3brdNum 5
/testjig/core/lhsFwdLogic/s3rdNum 5
/testjig/core/lhsFwdLogic/s4brdNum 5
/testjig/core/lhsFwdLogic/s4rdNum 5
/testjig/core/lhsFwdLogic/s5brdNum 5
/testjig/core/lhsFwdLogic/s5rdNum 5
/testjig/core/s1stall
/testjig/core/s2stall
/testjig/core/s3stalled
/testjig/core/s4stalled
/testjig/core/s5stalled
/testjig/core/s1bstall
/testjig/core/s2bstall
/testjig/core/s3bstalled
/testjig/core/s4bstalled
/testjig/core/s5bstalled
-
/testjig/core/lhsFwdLogic/regNum 00101
/testjig/core/lhsFwdLogic/s3rdNum 00101
/testjig/core/lhsFwdLogic/s4rdNum 00101
/testjig/core/lhsFwdLogic/s5rdNum 00101
/testjig/core/lhsFwdLogic/s3brdNum 00101
/testjig/core/lhsFwdLogic/s4brdNum 00101
/testjig/core/lhsFwdLogic/s5brdNum 00101
/testjig/core/lhsFwdLogic/s3stall
/testjig/core/lhsFwdLogic/s3bstall
58 us
60 us
62 us

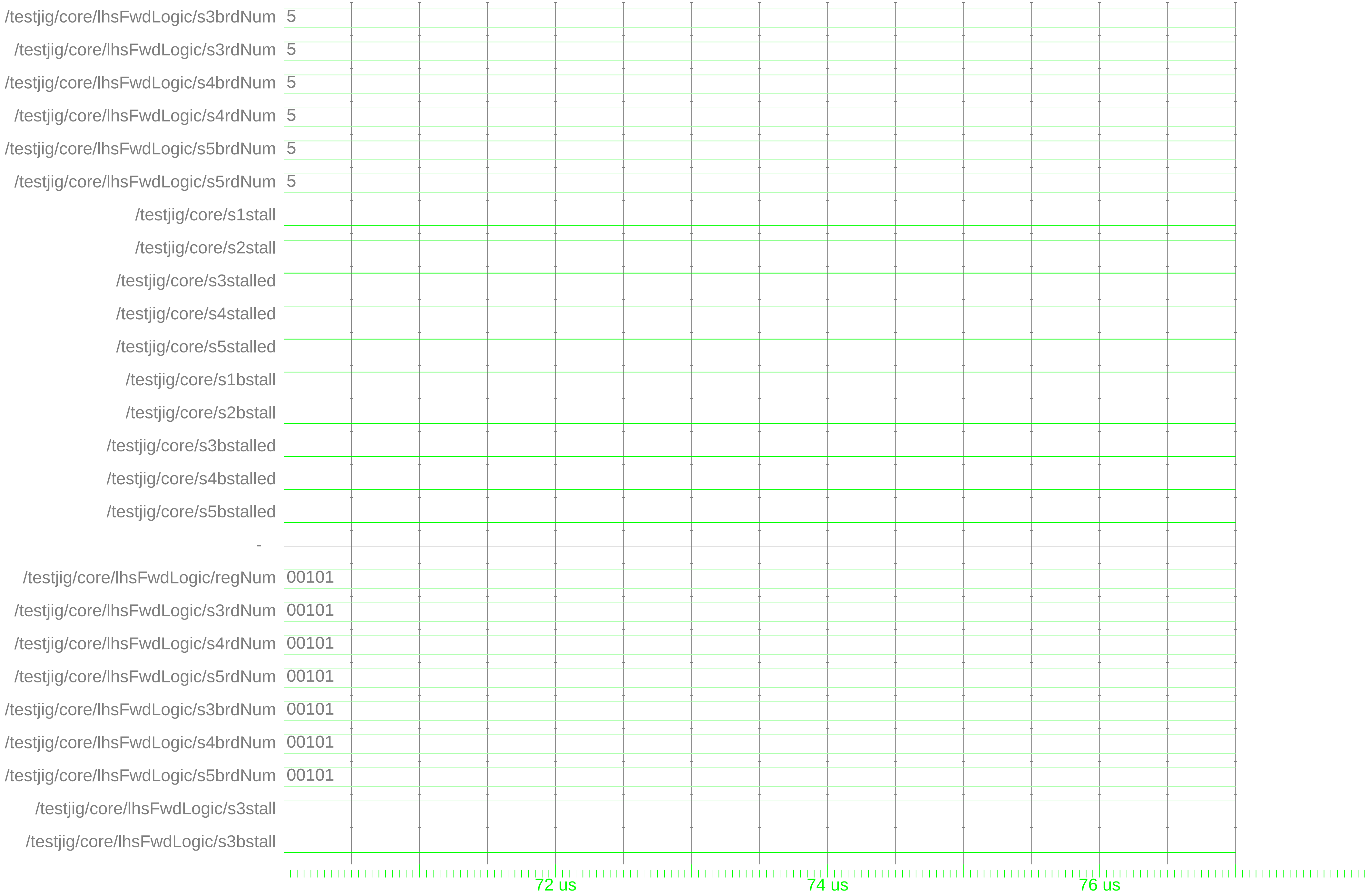

/testjig/core/lhsFwdLogic/s4stall
/testjig/core/lhsFwdLogic/s4bstall
/testjig/core/lhsFwdLogic/s5stall
/testjig/core/lhsFwdLogic/s5bstall
/testjig/core/lhsFwdLogic/s3doLoad
/testjig/core/lhsFwdLogic/fwdSel
010
/testjig/core/lhsFwdLogic/stall
/testjig/core/lhsFwdLogic/s3
/testjig/core/lhsFwdLogic/s3b
/testjig/core/lhsFwdLogic/s4
/testjig/core/lhsFwdLogic/s4b
/testjig/core/lhsFwdLogic/s5
/testjig/core/lhsFwdLogic/s5b
58 us
60 us
62 us

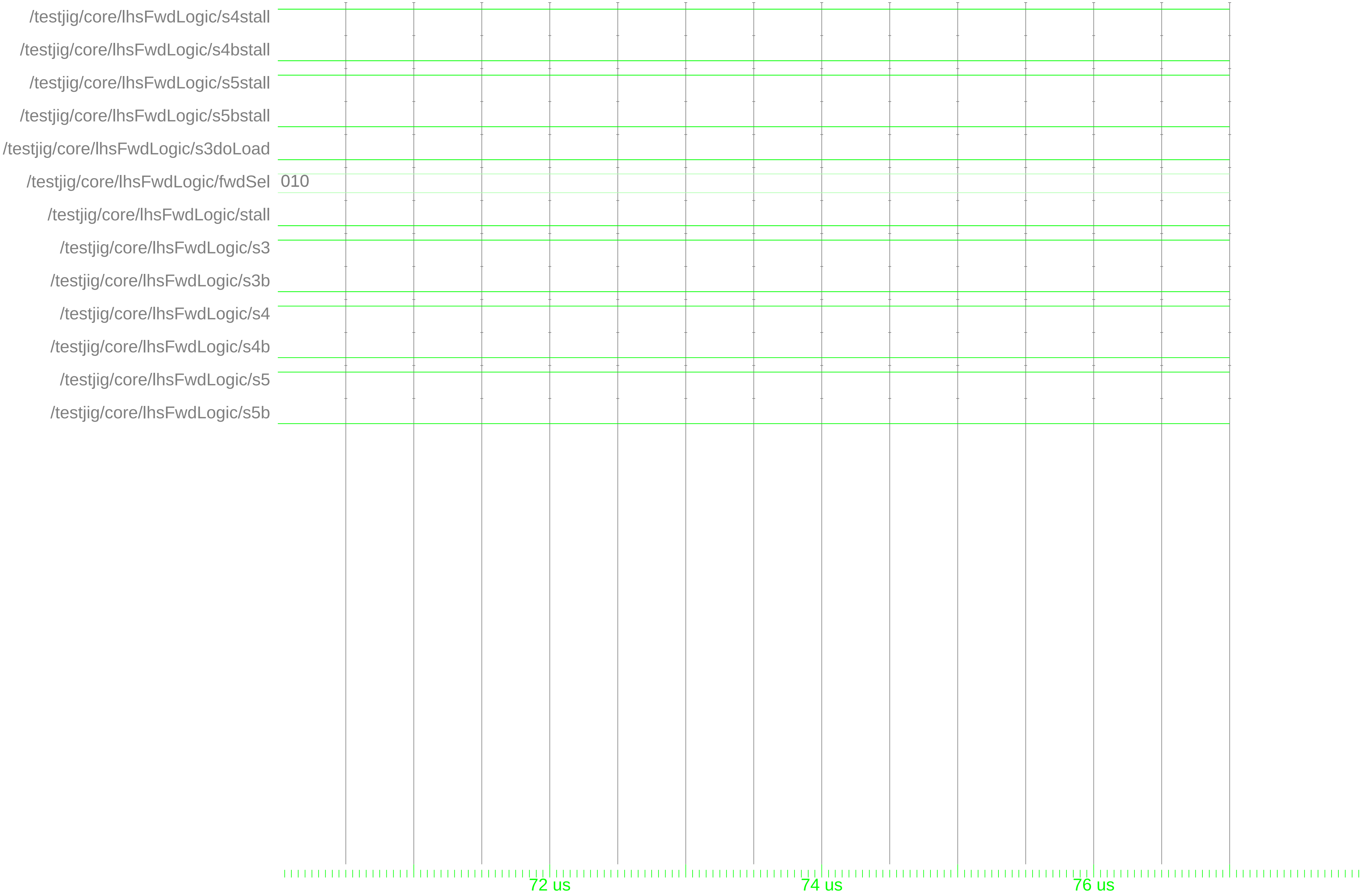

/testjig/core/clk
/testjig/core/pc
00400008
/testjig/core/s2isSysCall
/testjig/core/s2bisSysCall
/testjig/core/s3bisSysCall
/testjig/core/s3isSysCall
/testjig/core/s4bisSysCall
/testjig/core/s4isSysCall
/testjig/core/s5bisSysCall
/testjig/core/s5isSysCall
/testjig/core/s2r_v0
00000000
/testjig/core/s2binstMuxed
00c63820
/testjig/core/loadInterlock
/testjig/core/loadInterlockb
/testjig/core/s2pipeline2ok
/testjig/core/s3pipeline2ok
/testjig/core/lhsFwdLogic/s3
/testjig/core/lhsFwdLogic/s3b
/testjig/core/lhsFwdLogic/s4
/testjig/core/lhsFwdLogic/s4b
/testjig/core/lhsFwdLogic/s5
/testjig/core/lhsFwdLogic/s5b
/testjig/core/lhsFwdLogic/regNum
5
/testjig/core/rhsFwdLogic/regNum
5
/testjig/core/lhsFwdSel
010
/testjig/core/rhsFwdSel
010
64 us
66 us
68 us
70 us

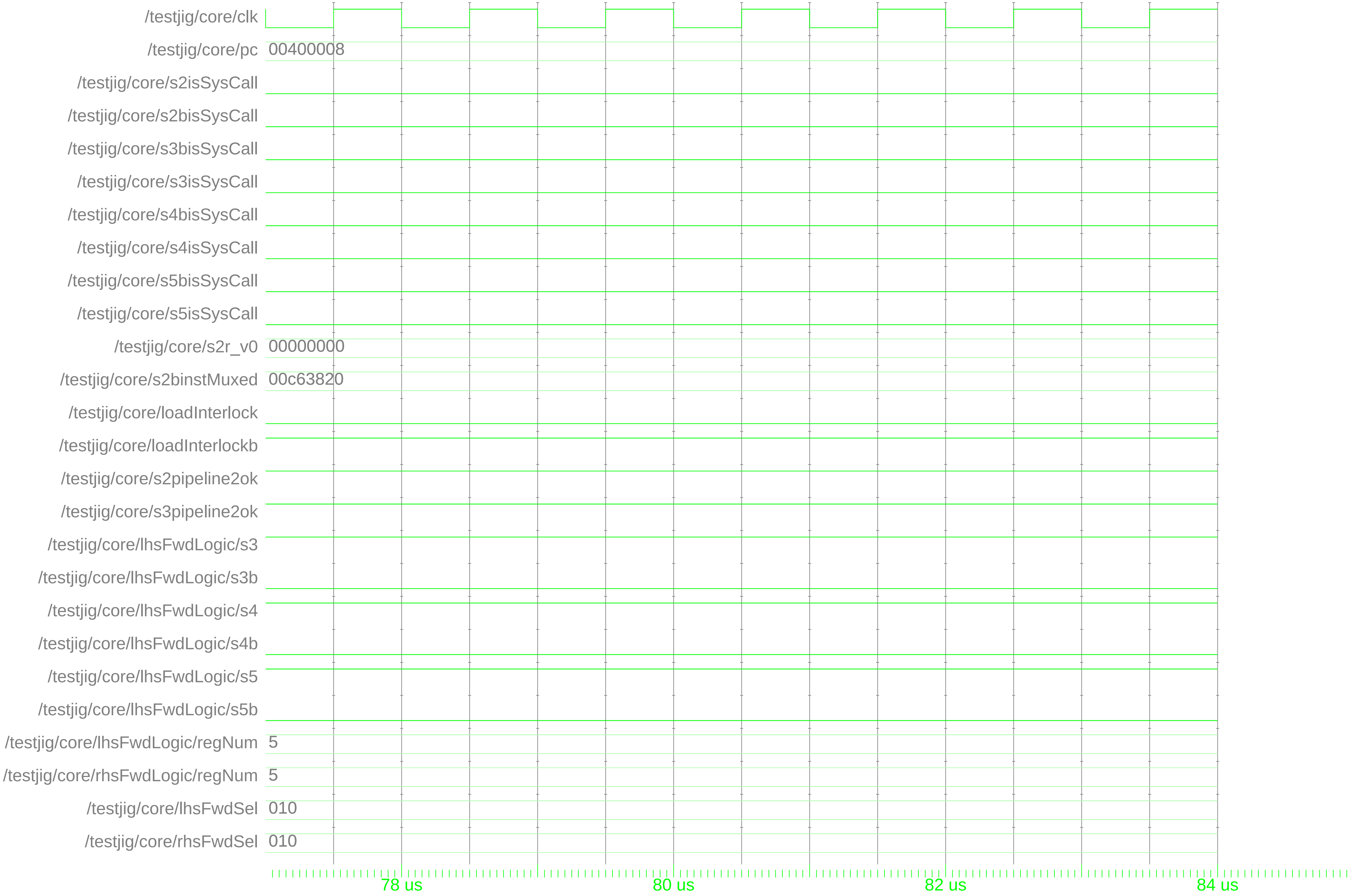

/testjig/core/lhsFwdLogic/s3brdNum 5
/testjig/core/lhsFwdLogic/s3rdNum 5
/testjig/core/lhsFwdLogic/s4brdNum 5
/testjig/core/lhsFwdLogic/s4rdNum 5
/testjig/core/lhsFwdLogic/s5brdNum 5
/testjig/core/lhsFwdLogic/s5rdNum 5
/testjig/core/s1stall
/testjig/core/s2stall
/testjig/core/s3stalled
/testjig/core/s4stalled
/testjig/core/s5stalled
/testjig/core/s1bstall
/testjig/core/s2bstall
/testjig/core/s3bstalled
/testjig/core/s4bstalled
/testjig/core/s5bstalled
-
/testjig/core/lhsFwdLogic/regNum 00101
/testjig/core/lhsFwdLogic/s3rdNum 00101
/testjig/core/lhsFwdLogic/s4rdNum 00101
/testjig/core/lhsFwdLogic/s5rdNum 00101
/testjig/core/lhsFwdLogic/s3brdNum 00101
/testjig/core/lhsFwdLogic/s4brdNum 00101
/testjig/core/lhsFwdLogic/s5brdNum 00101
/testjig/core/lhsFwdLogic/s3stall
/testjig/core/lhsFwdLogic/s3bstall
64 us
66 us
68 us
70 us

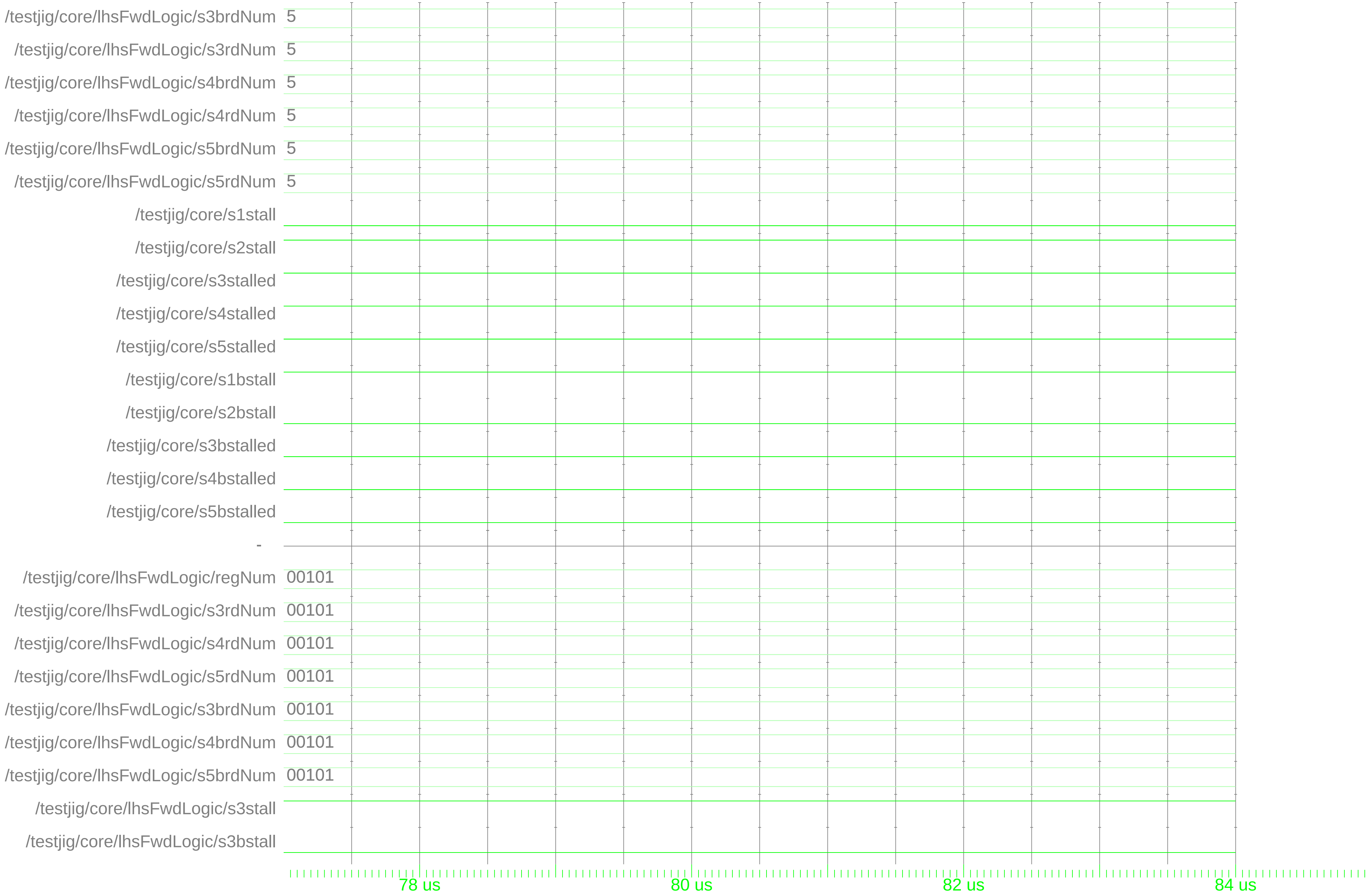

/testjig/core/lhsFwdLogic/s4stall
/testjig/core/lhsFwdLogic/s4bstall
/testjig/core/lhsFwdLogic/s5stall
/testjig/core/lhsFwdLogic/s5bstall
/testjig/core/lhsFwdLogic/s3doLoad
/testjig/core/lhsFwdLogic/fwdSel
010
/testjig/core/lhsFwdLogic/stall
/testjig/core/lhsFwdLogic/s3
/testjig/core/lhsFwdLogic/s3b
/testjig/core/lhsFwdLogic/s4
/testjig/core/lhsFwdLogic/s4b
/testjig/core/lhsFwdLogic/s5
/testjig/core/lhsFwdLogic/s5b
64 us
66 us
68 us
70 us

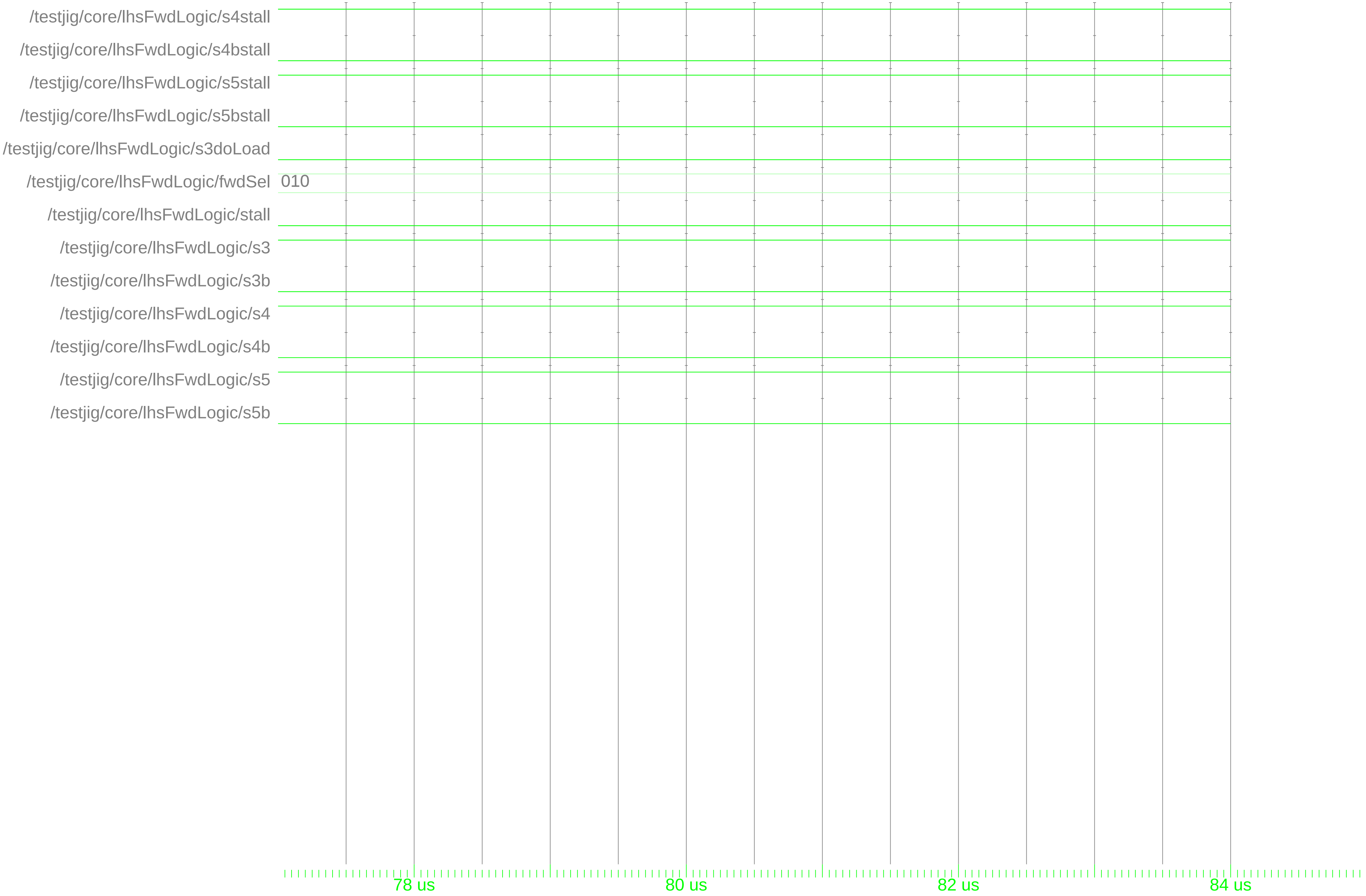

/testjig/core/clk
/testjig/core/pc
00400008
/testjig/core/s2isSysCall
/testjig/core/s2bisSysCall
/testjig/core/s3bisSysCall
/testjig/core/s3isSysCall
/testjig/core/s4bisSysCall
/testjig/core/s4isSysCall
/testjig/core/s5bisSysCall
/testjig/core/s5isSysCall
/testjig/core/s2r_v0
00000000
/testjig/core/s2binstMuxed
00c63820
/testjig/core/loadInterlock
/testjig/core/loadInterlockb
/testjig/core/s2pipeline2ok
/testjig/core/s3pipeline2ok
/testjig/core/lhsFwdLogic/s3
/testjig/core/lhsFwdLogic/s3b
/testjig/core/lhsFwdLogic/s4
/testjig/core/lhsFwdLogic/s4b
/testjig/core/lhsFwdLogic/s5
/testjig/core/lhsFwdLogic/s5b
/testjig/core/lhsFwdLogic/regNum
5
/testjig/core/rhsFwdLogic/regNum
5
/testjig/core/lhsFwdSel
010
/testjig/core/rhsFwdSel
010
72 us
74 us
76 us

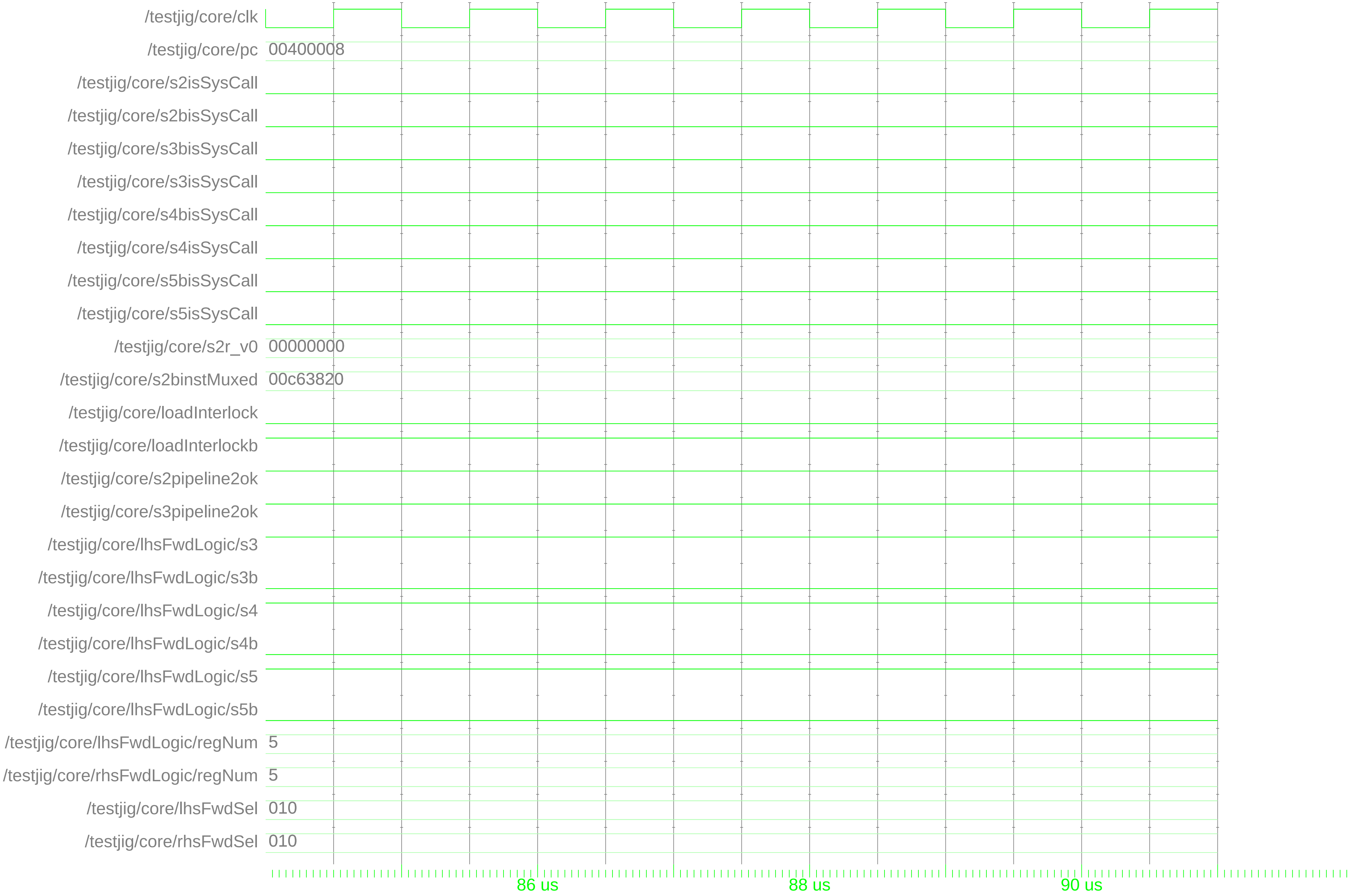

/testjig/core/lhsFwdLogic/s3brdNum 5
/testjig/core/lhsFwdLogic/s3rdNum 5
/testjig/core/lhsFwdLogic/s4brdNum 5
/testjig/core/lhsFwdLogic/s4rdNum 5
/testjig/core/lhsFwdLogic/s5brdNum 5
/testjig/core/lhsFwdLogic/s5rdNum 5
/testjig/core/s1stall
/testjig/core/s2stall
/testjig/core/s3stalled
/testjig/core/s4stalled
/testjig/core/s5stalled
/testjig/core/s1bstall
/testjig/core/s2bstall
/testjig/core/s3bstalled
/testjig/core/s4bstalled
/testjig/core/s5bstalled
-
/testjig/core/lhsFwdLogic/regNum 00101
/testjig/core/lhsFwdLogic/s3rdNum 00101
/testjig/core/lhsFwdLogic/s4rdNum 00101
/testjig/core/lhsFwdLogic/s5rdNum 00101
/testjig/core/lhsFwdLogic/s3brdNum 00101
/testjig/core/lhsFwdLogic/s4brdNum 00101
/testjig/core/lhsFwdLogic/s5brdNum 00101
/testjig/core/lhsFwdLogic/s3stall
/testjig/core/lhsFwdLogic/s3bstall
72 us
74 us
76 us

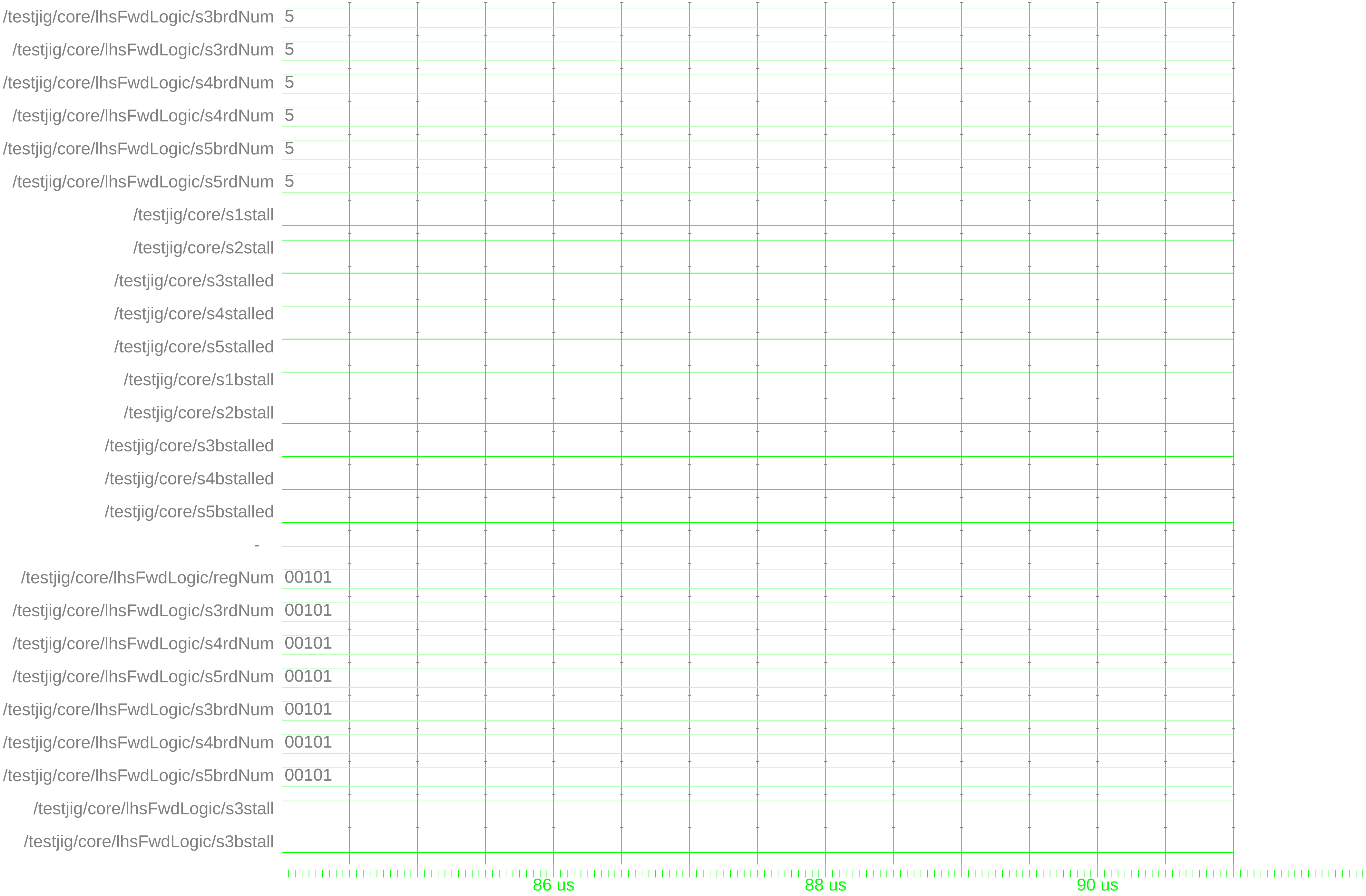

/testjig/core/lhsFwdLogic/s4stall
/testjig/core/lhsFwdLogic/s4bstall
/testjig/core/lhsFwdLogic/s5stall
/testjig/core/lhsFwdLogic/s5bstall
/testjig/core/lhsFwdLogic/s3doLoad
/testjig/core/lhsFwdLogic/fwdSel
010
/testjig/core/lhsFwdLogic/stall
/testjig/core/lhsFwdLogic/s3
/testjig/core/lhsFwdLogic/s3b
/testjig/core/lhsFwdLogic/s4
/testjig/core/lhsFwdLogic/s4b
/testjig/core/lhsFwdLogic/s5
/testjig/core/lhsFwdLogic/s5b
72 us
74 us
76 us

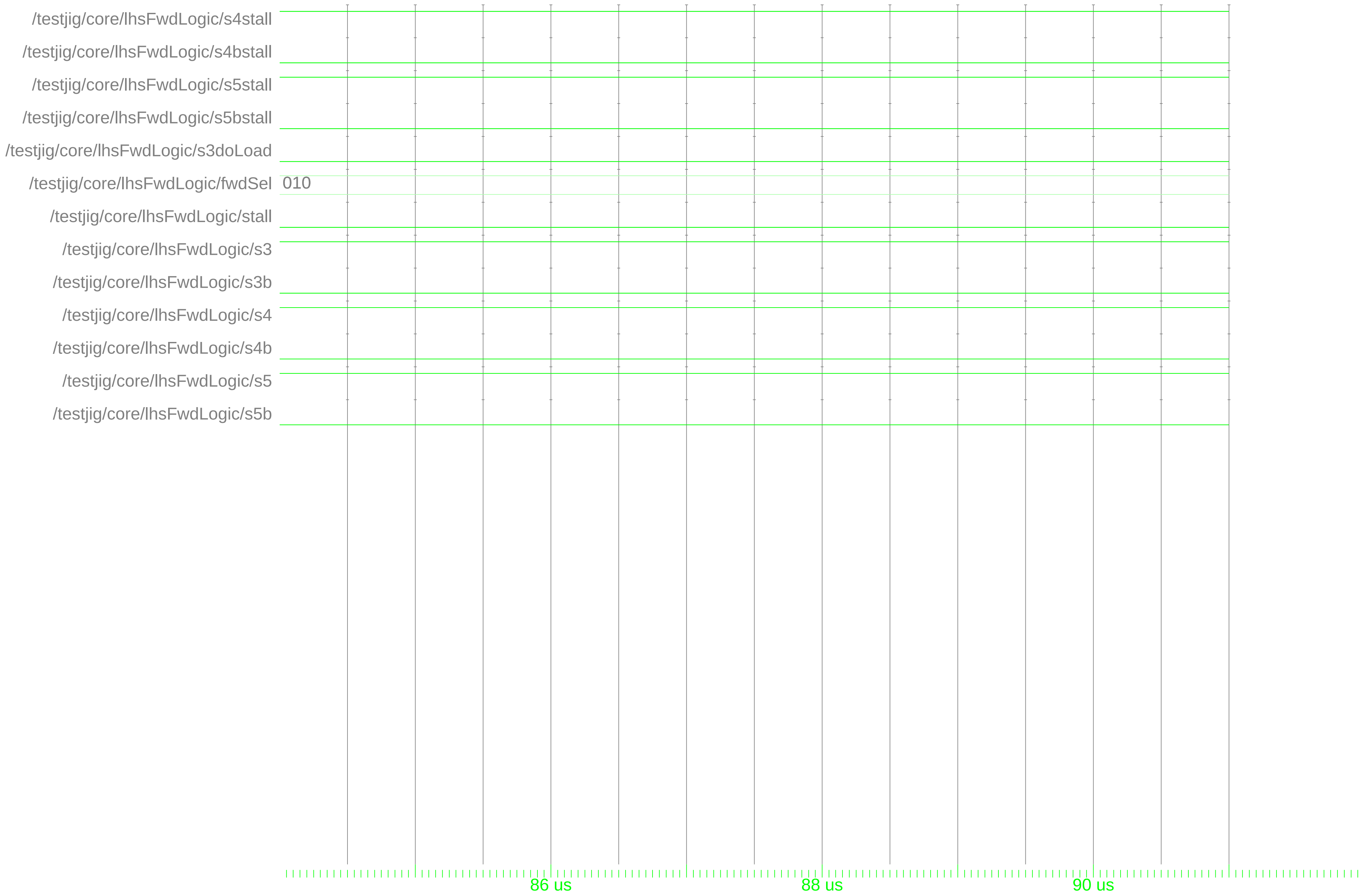

/testjig/core/clk
/testjig/core/pc 00400008
/testjig/core/s2isSysCall
/testjig/core/s2bisSysCall
/testjig/core/s3bisSysCall
/testjig/core/s3isSysCall
/testjig/core/s4bisSysCall
/testjig/core/s4isSysCall
/testjig/core/s5bisSysCall
/testjig/core/s5isSysCall
/testjig/core/s2r_v0 00000000
/testjig/core/s2binstMuxed 00c63820
/testjig/core/loadInterlock
/testjig/core/loadInterlockb
/testjig/core/s2pipeline2ok
/testjig/core/s3pipeline2ok
/testjig/core/lhsFwdLogic/s3
/testjig/core/lhsFwdLogic/s3b
/testjig/core/lhsFwdLogic/s4
/testjig/core/lhsFwdLogic/s4b
/testjig/core/lhsFwdLogic/s5
/testjig/core/lhsFwdLogic/s5b
/testjig/core/lhsFwdLogic/regNum 5
/testjig/core/rhsFwdLogic/regNum 5
/testjig/core/lhsFwdSel 010
/testjig/core/rhsFwdSel 010
78 us
80 us
82 us
84 us

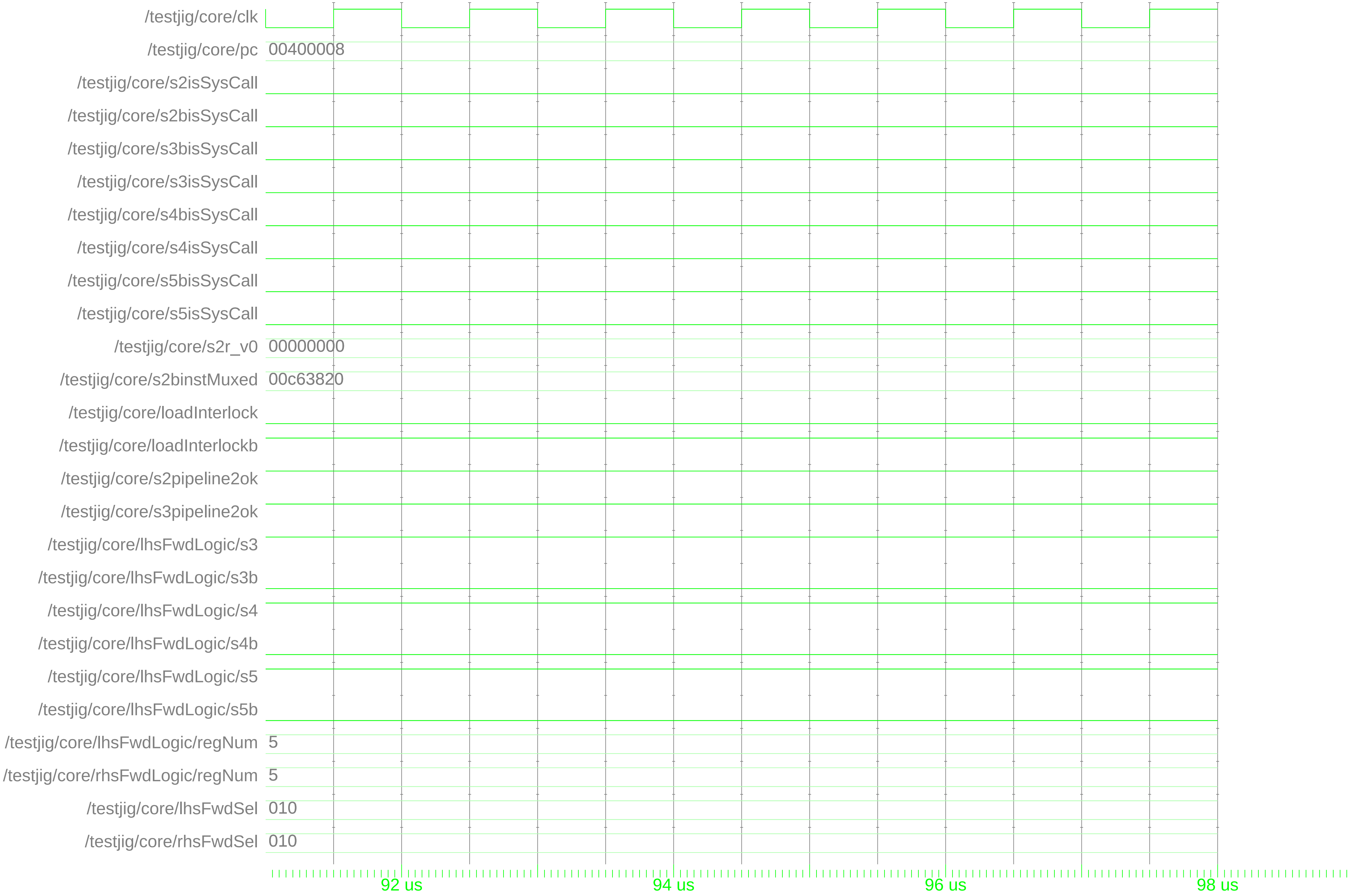

/testjig/core/lhsFwdLogic/s3brdNum 5
/testjig/core/lhsFwdLogic/s3rdNum 5
/testjig/core/lhsFwdLogic/s4brdNum 5
/testjig/core/lhsFwdLogic/s4rdNum 5
/testjig/core/lhsFwdLogic/s5brdNum 5
/testjig/core/lhsFwdLogic/s5rdNum 5
/testjig/core/s1stall
/testjig/core/s2stall
/testjig/core/s3stalled
/testjig/core/s4stalled
/testjig/core/s5stalled
/testjig/core/s1bstall
/testjig/core/s2bstall
/testjig/core/s3bstalled
/testjig/core/s4bstalled
/testjig/core/s5bstalled
-
/testjig/core/lhsFwdLogic/regNum 00101
/testjig/core/lhsFwdLogic/s3rdNum 00101
/testjig/core/lhsFwdLogic/s4rdNum 00101
/testjig/core/lhsFwdLogic/s5rdNum 00101
/testjig/core/lhsFwdLogic/s3brdNum 00101
/testjig/core/lhsFwdLogic/s4brdNum 00101
/testjig/core/lhsFwdLogic/s5brdNum 00101
/testjig/core/lhsFwdLogic/s3stall
/testjig/core/lhsFwdLogic/s3bstall
78 us
80 us
82 us
84 us


/testjig/core/lhsFwdLogic/s4stall
/testjig/core/lhsFwdLogic/s4bstall
/testjig/core/lhsFwdLogic/s5stall
/testjig/core/lhsFwdLogic/s5bstall
/testjig/core/lhsFwdLogic/s3doLoad
/testjig/core/lhsFwdLogic/fwdSel
010
/testjig/core/lhsFwdLogic/stall
/testjig/core/lhsFwdLogic/s3
/testjig/core/lhsFwdLogic/s3b
/testjig/core/lhsFwdLogic/s4
/testjig/core/lhsFwdLogic/s4b
/testjig/core/lhsFwdLogic/s5
/testjig/core/lhsFwdLogic/s5b
78 us
80 us
82 us
84 us

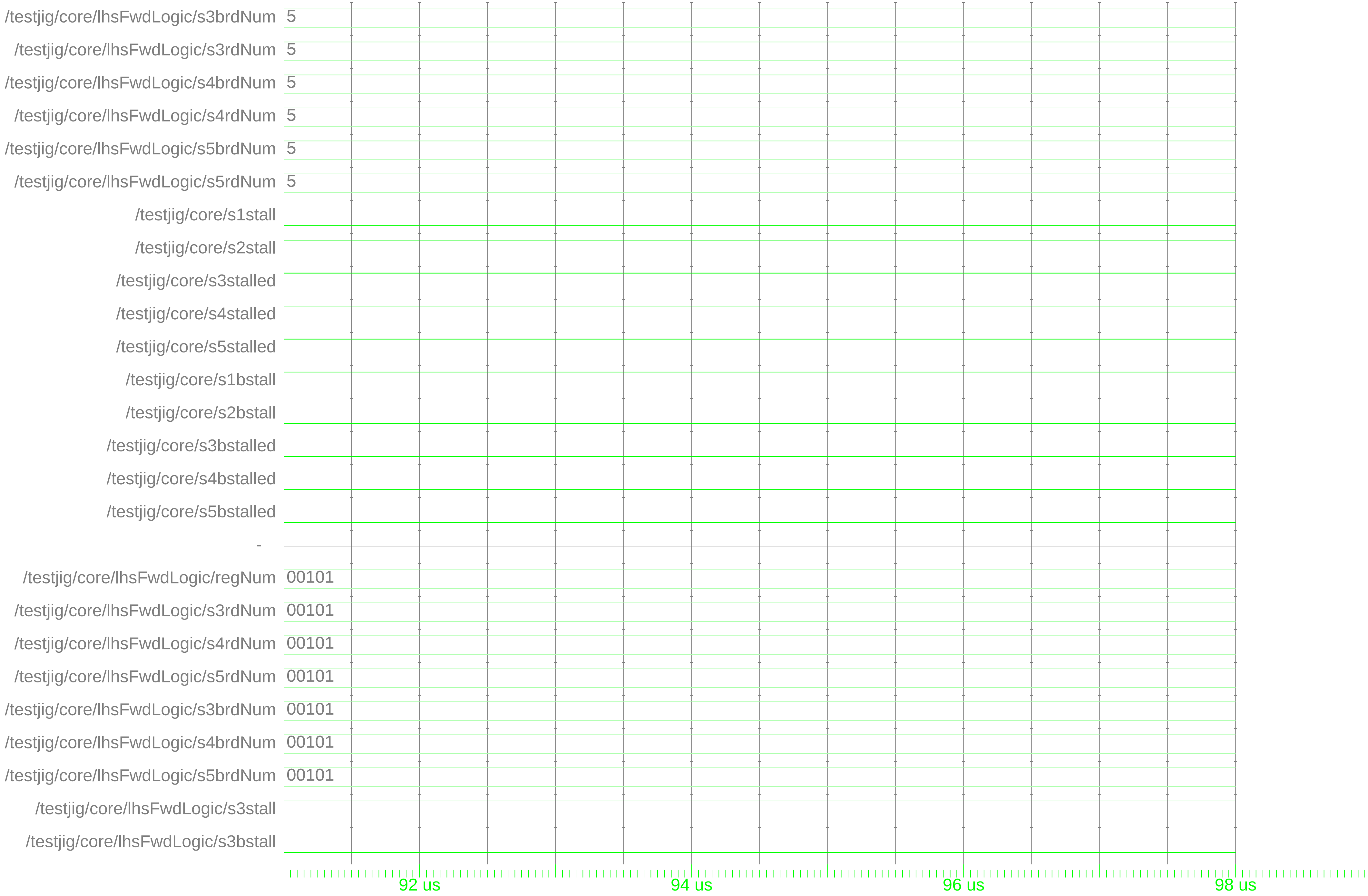

/testjig/core/clk
/testjig/core/pc
00400008
/testjig/core/s2isSysCall
/testjig/core/s2bisSysCall
/testjig/core/s3bisSysCall
/testjig/core/s3isSysCall
/testjig/core/s4bisSysCall
/testjig/core/s4isSysCall
/testjig/core/s5bisSysCall
/testjig/core/s5isSysCall
/testjig/core/s2r_v0
00000000
/testjig/core/s2binstMuxed
00c63820
/testjig/core/loadInterlock
/testjig/core/loadInterlockb
/testjig/core/s2pipeline2ok
/testjig/core/s3pipeline2ok
/testjig/core/lhsFwdLogic/s3
/testjig/core/lhsFwdLogic/s3b
/testjig/core/lhsFwdLogic/s4
/testjig/core/lhsFwdLogic/s4b
/testjig/core/lhsFwdLogic/s5
/testjig/core/lhsFwdLogic/s5b
/testjig/core/lhsFwdLogic/regNum
5
/testjig/core/rhsFwdLogic/regNum
5
/testjig/core/lhsFwdSel
010
/testjig/core/rhsFwdSel
010
86 us
88 us
90 us

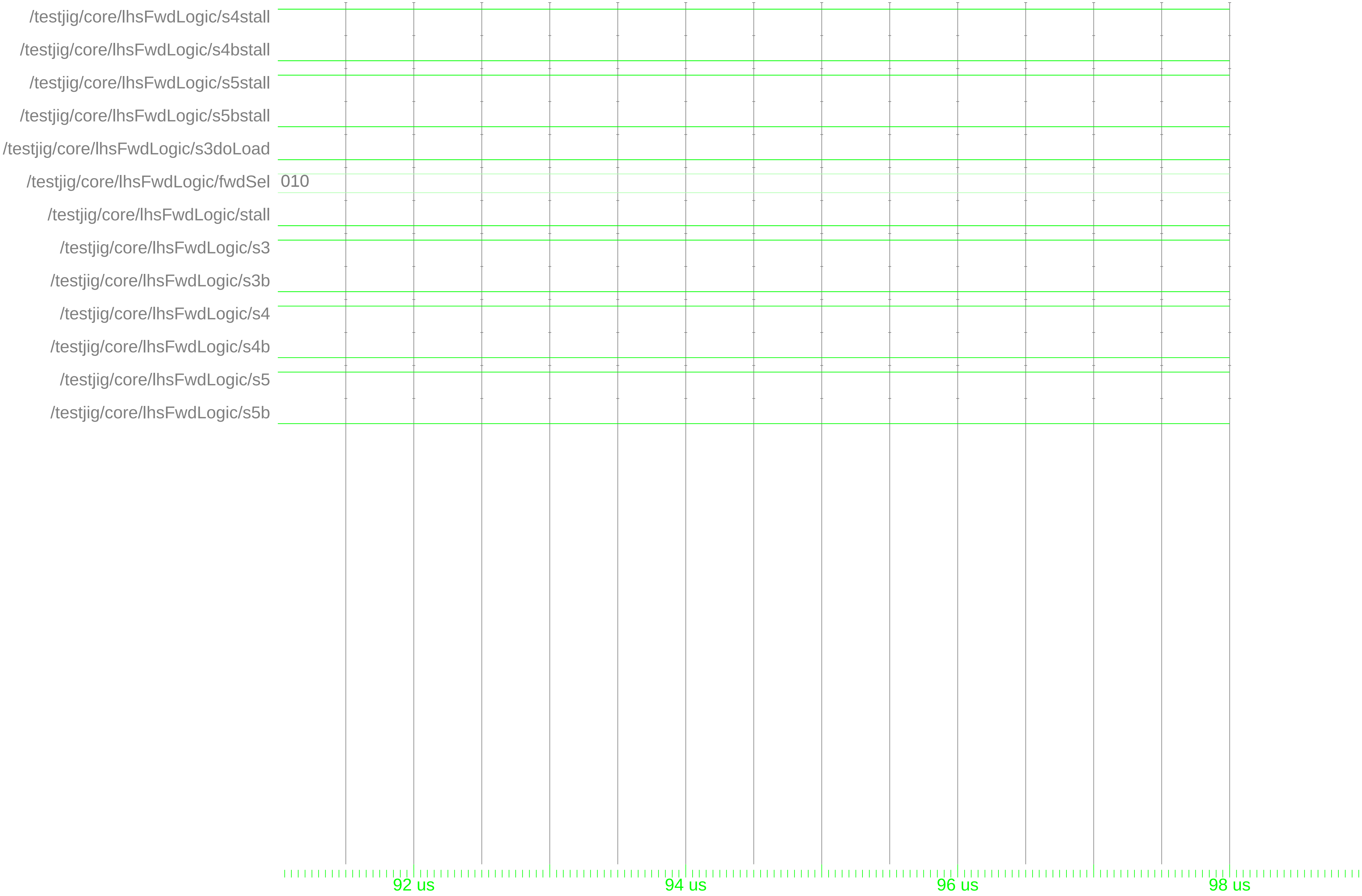

/testjig/core/lhsFwdLogic/s3brdNum 5
/testjig/core/lhsFwdLogic/s3rdNum 5
/testjig/core/lhsFwdLogic/s4brdNum 5
/testjig/core/lhsFwdLogic/s4rdNum 5
/testjig/core/lhsFwdLogic/s5brdNum 5
/testjig/core/lhsFwdLogic/s5rdNum 5
/testjig/core/s1stall
/testjig/core/s2stall
/testjig/core/s3stalled
/testjig/core/s4stalled
/testjig/core/s5stalled
/testjig/core/s1bstall
/testjig/core/s2bstall
/testjig/core/s3bstalled
/testjig/core/s4bstalled
/testjig/core/s5bstalled
-
/testjig/core/lhsFwdLogic/regNum 00101
/testjig/core/lhsFwdLogic/s3rdNum 00101
/testjig/core/lhsFwdLogic/s4rdNum 00101
/testjig/core/lhsFwdLogic/s5rdNum 00101
/testjig/core/lhsFwdLogic/s3brdNum 00101
/testjig/core/lhsFwdLogic/s4brdNum 00101
/testjig/core/lhsFwdLogic/s5brdNum 00101
/testjig/core/lhsFwdLogic/s3stall
/testjig/core/lhsFwdLogic/s3bstall
86 us
88 us
90 us

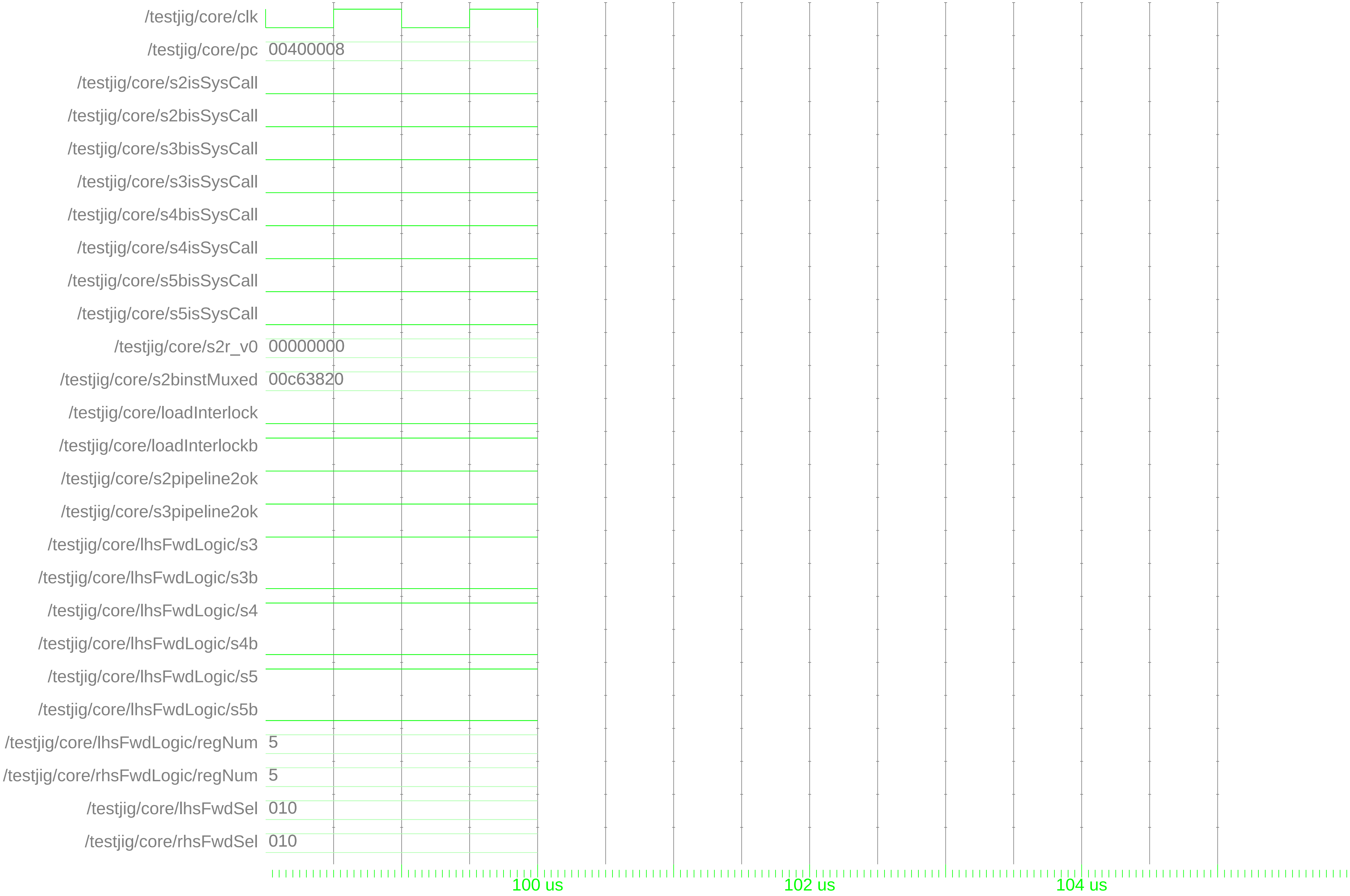

/testjig/core/lhsFwdLogic/s4stall
/testjig/core/lhsFwdLogic/s4bstall
/testjig/core/lhsFwdLogic/s5stall
/testjig/core/lhsFwdLogic/s5bstall
/testjig/core/lhsFwdLogic/s3doLoad
/testjig/core/lhsFwdLogic/fwdSel
010
/testjig/core/lhsFwdLogic/stall
/testjig/core/lhsFwdLogic/s3
/testjig/core/lhsFwdLogic/s3b
/testjig/core/lhsFwdLogic/s4
/testjig/core/lhsFwdLogic/s4b
/testjig/core/lhsFwdLogic/s5
/testjig/core/lhsFwdLogic/s5b
86 us
88 us
90 us



Entity:testjig Architecture: Date: Sat Dec 06 09:27:30 EST 2003 Row: 14 Page: 40


/testjig/core/lhsFwdLogic/s3brdNum 5
/testjig/core/lhsFwdLogic/s3rdNum 5
/testjig/core/lhsFwdLogic/s4brdNum 5
/testjig/core/lhsFwdLogic/s4rdNum 5
/testjig/core/lhsFwdLogic/s5brdNum 5
/testjig/core/lhsFwdLogic/s5rdNum 5
/testjig/core/s1stall
/testjig/core/s2stall
/testjig/core/s3stalled
/testjig/core/s4stalled
/testjig/core/s5stalled
/testjig/core/s1bstall
/testjig/core/s2bstall
/testjig/core/s3bstalled
/testjig/core/s4bstalled
/testjig/core/s5bstalled
-
/testjig/core/lhsFwdLogic/regNum 00101
/testjig/core/lhsFwdLogic/s3rdNum 00101
/testjig/core/lhsFwdLogic/s4rdNum 00101
/testjig/core/lhsFwdLogic/s5rdNum 00101
/testjig/core/lhsFwdLogic/s3brdNum 00101
/testjig/core/lhsFwdLogic/s4brdNum 00101
/testjig/core/lhsFwdLogic/s5brdNum 00101
/testjig/core/lhsFwdLogic/s3stall
/testjig/core/lhsFwdLogic/s3bstall
92 us
94 us
96 us
98 us


/testjig/core/lhsFwdLogic/s4stall
/testjig/core/lhsFwdLogic/s4bstall
/testjig/core/lhsFwdLogic/s5stall
/testjig/core/lhsFwdLogic/s5bstall
/testjig/core/lhsFwdLogic/s3doLoad
/testjig/core/lhsFwdLogic/fwdSel
010
/testjig/core/lhsFwdLogic/stall
/testjig/core/lhsFwdLogic/s3
/testjig/core/lhsFwdLogic/s3b
/testjig/core/lhsFwdLogic/s4
/testjig/core/lhsFwdLogic/s4b
/testjig/core/lhsFwdLogic/s5
/testjig/core/lhsFwdLogic/s5b
92 us
94 us
96 us
98 us


/testjig/core/clk
/testjig/core/pc
00400008
/testjig/core/s2isSysCall
/testjig/core/s2bisSysCall
/testjig/core/s3bisSysCall
/testjig/core/s3isSysCall
/testjig/core/s4bisSysCall
/testjig/core/s4isSysCall
/testjig/core/s5bisSysCall
/testjig/core/s5isSysCall
/testjig/core/s2r_v0
00000000
/testjig/core/s2binstMuxed
00c63820
/testjig/core/loadInterlock
/testjig/core/loadInterlockb
/testjig/core/s2pipeline2ok
/testjig/core/s3pipeline2ok
/testjig/core/lhsFwdLogic/s3
/testjig/core/lhsFwdLogic/s3b
/testjig/core/lhsFwdLogic/s4
/testjig/core/lhsFwdLogic/s4b
/testjig/core/lhsFwdLogic/s5
/testjig/core/lhsFwdLogic/s5b
/testjig/core/lhsFwdLogic/regNum
5
/testjig/core/rhsFwdLogic/regNum
5
/testjig/core/lhsFwdSel
010
/testjig/core/rhsFwdSel
010
100 us
102 us
104 us


/testjig/core/lhsFwdLogic/s3brdNum 5
/testjig/core/lhsFwdLogic/s3rdNum 5
/testjig/core/lhsFwdLogic/s4brdNum 5
/testjig/core/lhsFwdLogic/s4rdNum 5
/testjig/core/lhsFwdLogic/s5brdNum 5
/testjig/core/lhsFwdLogic/s5rdNum 5
/testjig/core/s1stall
/testjig/core/s2stall
/testjig/core/s3stalled
/testjig/core/s4stalled
/testjig/core/s5stalled
/testjig/core/s1bstall
/testjig/core/s2bstall
/testjig/core/s3bstalled
/testjig/core/s4bstalled
/testjig/core/s5bstalled
-
/testjig/core/lhsFwdLogic/regNum 00101
/testjig/core/lhsFwdLogic/s3rdNum 00101
/testjig/core/lhsFwdLogic/s4rdNum 00101
/testjig/core/lhsFwdLogic/s5rdNum 00101
/testjig/core/lhsFwdLogic/s3brdNum 00101
/testjig/core/lhsFwdLogic/s4brdNum 00101
/testjig/core/lhsFwdLogic/s5brdNum 00101
/testjig/core/lhsFwdLogic/s3stall
/testjig/core/lhsFwdLogic/s3bstall
100 us
102 us
104 us


/testjig/core/lhsFwdLogic/s4stall
/testjig/core/lhsFwdLogic/s4bstall
/testjig/core/lhsFwdLogic/s5stall
/testjig/core/lhsFwdLogic/s5bstall
/testjig/core/lhsFwdLogic/s3doLoad
/testjig/core/lhsFwdLogic/fwdSel
010
/testjig/core/lhsFwdLogic/stall
/testjig/core/lhsFwdLogic/s3
/testjig/core/lhsFwdLogic/s3b
/testjig/core/lhsFwdLogic/s4
/testjig/core/lhsFwdLogic/s4b
/testjig/core/lhsFwdLogic/s5
/testjig/core/lhsFwdLogic/s5b
100 us
102 us
104 us